Innovative Satellite On-Board Data Handling Techniques

CEOI Innovations in Remote Sensing Event
Hamilton House, London WC1
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All the space you need

ASTRIUM
AN EADS COMPANY

Introduction

Context

- On-board processing for spaceborne EO Instruments

Motivation

- Fully exploit latest sensor capabilities
- Utilise latest reconfigurable DSP hardware technology

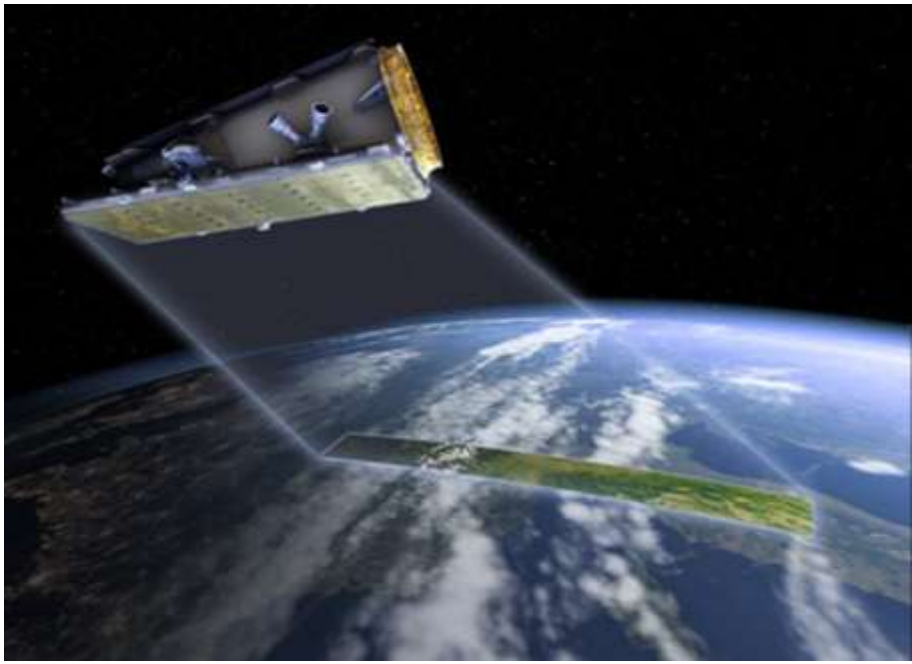
Opportunity

- Very high performance on-board processing
  - new applications and services
- Shared processing for multi-instrument payloads
  - potential savings in mass, power and programme cost

Case Study: Spaceborne Synthetic Aperture Radar

- Current spaceborne SAR processors
  - capture radar return
  - digitise waveforms
  - store in mass memory
  - transmit data to ground
- Technical challenges include
  - ADCs (12 bit, 3 GHz sampling)
  - SSMM (6 Tbit,1 Gbps read//write)

NovaSAR-S (SSTL, Astrium Ltd)



- Image processing performed in Ground Segment

BAE SYSTEMS

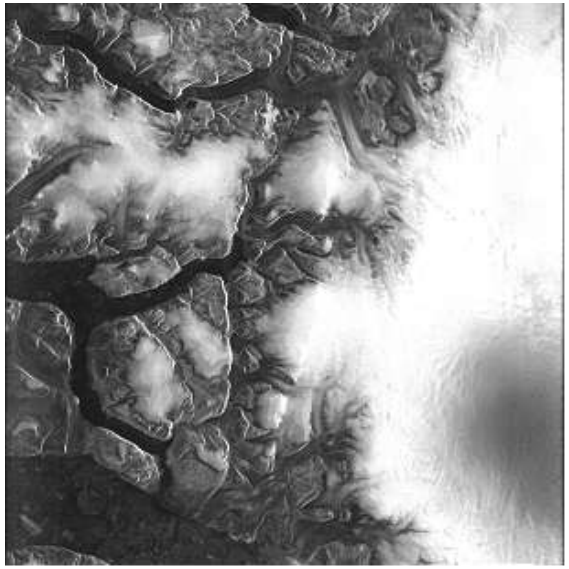
Centre for eo Instrumentation

CEOI 4th Call and 5th Call Seedcorn Studies

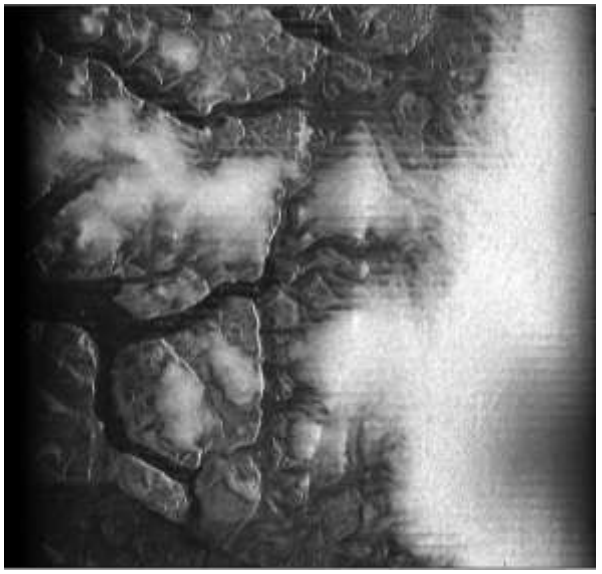
- On-board processing to generate SAR images
- Primary rationale is real time dissemination of imagery direct to users
  - met-ocean data for ship navigation
  - offshore engineering (oil and gas platforms)
  - weather forecasting
  - sea ice products for navigation and disaster monitoring (earthquakes, floods, forest fires, oil spills)
- Image formation requires high performance hardware
  - computationally intensive DSP algorithms

CEOI 4th Call and 5th Call Seedcorn Studies

Greenland ERS-2 dataset (21st March 2011 Orbit 83218, Frame 1909, 16:26:42 UT (Descending))
Image orientation: near range at right and early azimuth at top

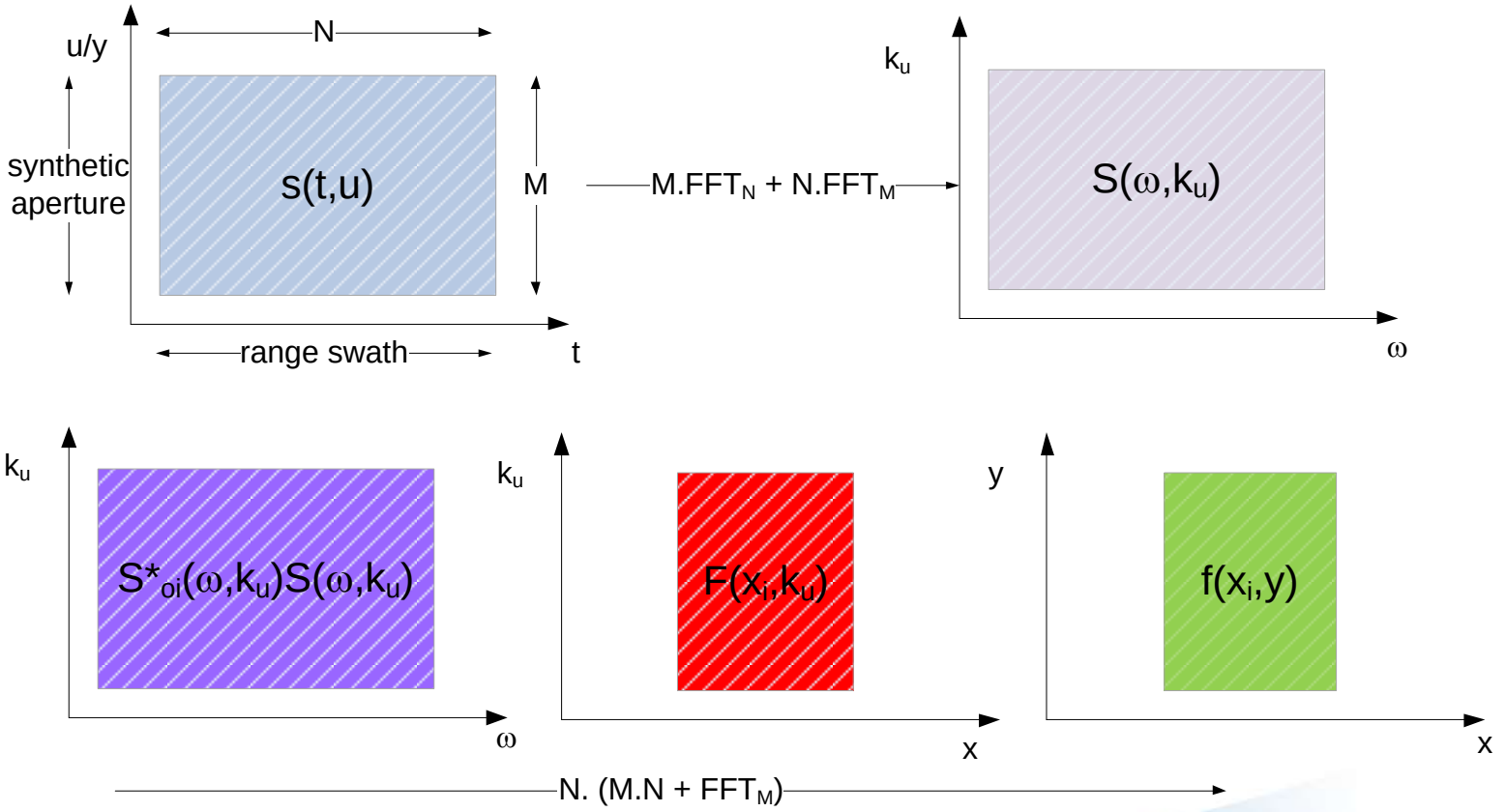


ESA SAR software



Trial image using range stacking algorithm

SAR Image Reconstruction: Algorithm



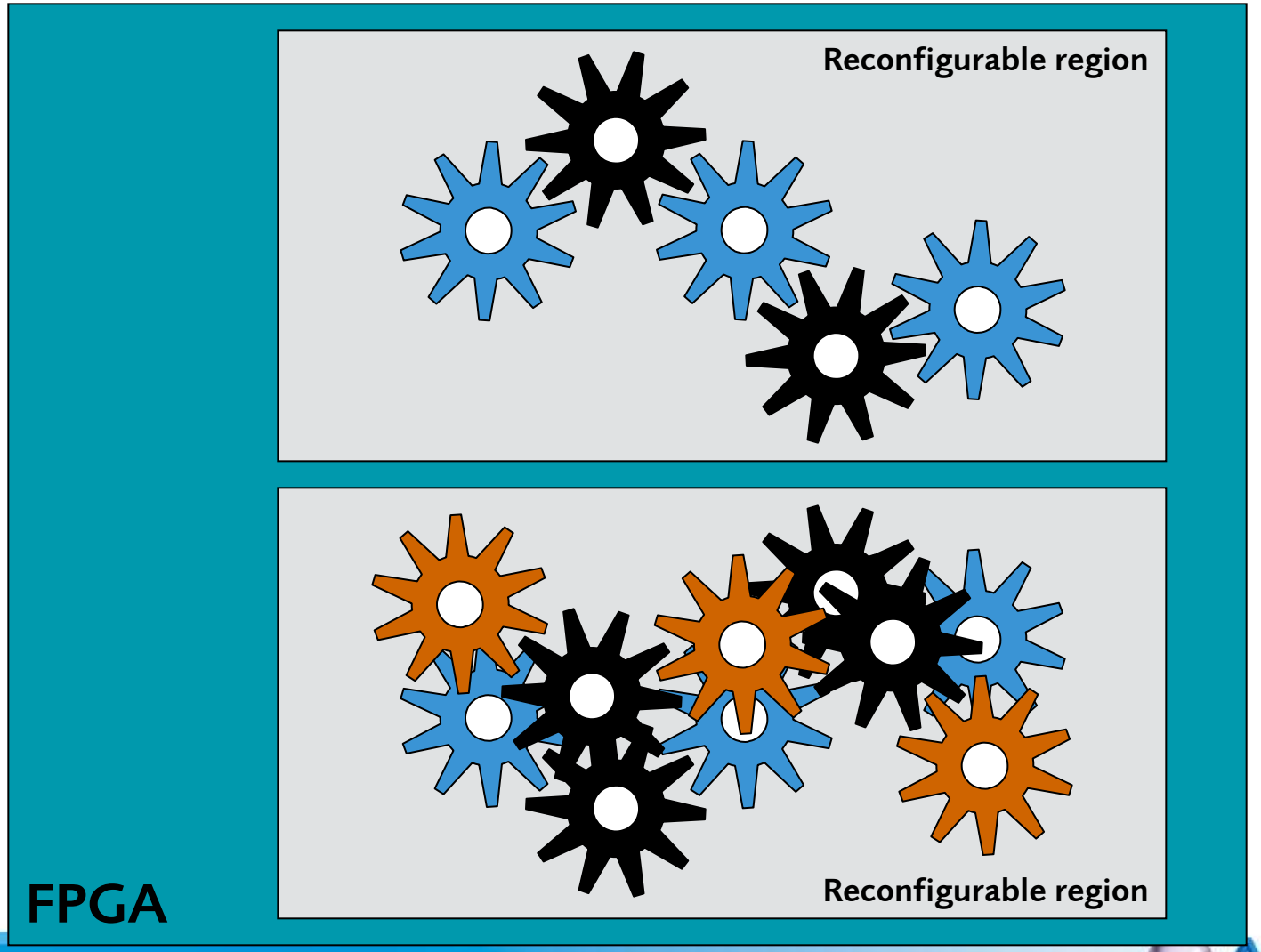
SAR Image Reconstruction: Computation Rate

- Multiplications/second ~ Pulse Repetition Frequency x N^2
  - PRF = 1680
  - N = 5616
  - multiplication rate ~ 5.10^{10}
- QML Virtex 5 FPGA:
  - dynamically reconfigurable
  - 320 multipliers
  - 200 MHz clock
  - multiplication rate ~ 6.10^{10}

Dynamically Reconfigurable Hardware

- Demonstrator developed for ESA by Astrium Ltd and IDA (Technical University of Brunswick)
- Architecture features
  - reconfigurable FPGAs for DSP
  - anti-fuse FPGA for SEU hard control
  - non-volatile (FLASH),volatile (SDRAM) memory
  - LEON cpu for control and management functions
  - high speed I/O to instrument front ends
- High capacity processing, shareable by multiple instruments

Dynamic, Partial Hardware Reconfiguration



UKSA SpaceCiti I-PDHS

EGSE (Platform Avionics OBC)

TC/TM

DRPM System

SpaceWire Router

System Controller (LEON-2FT)

NAND FLASH (Non Volatile Memory)

Configuration Controller (LEON-3)

SDRAM (Volatile Memory)

SOCWire Switch

RFPGA (Xilinx LX100)

RFGPA (Xilinx SX55)

DFPGA

MAG Front End

Camera Front End

Pender LEON-3 FT (IMA)

SpaceWire link

SOCWire link

Summary

- New instrument sensors require more on-board processing
- New processor technology enables greater sophistication and complexity in on-board data handling
- Innovative combinations of sensor and processor technologies offer new capabilities and services
- Technology could be relevant to non-space systems