Fully Depleted, Monolithic Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias

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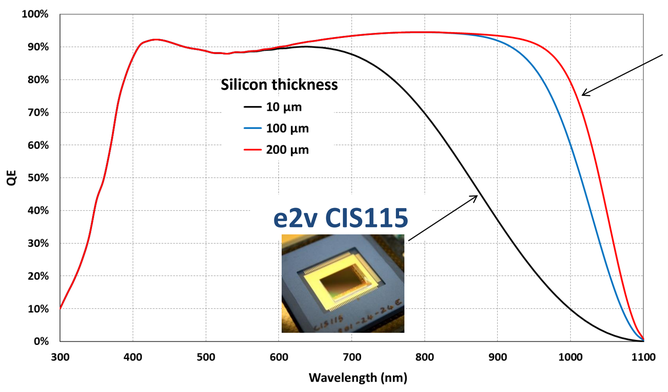
Summary

A new pixel design using fully depleted pinned photodiode (PPD) in a 180 nm monolithic CMOS image sensor (CIS) process has been developed as a proof of principle. The sensor can be fully depleted by means of reverse bias applied to the substrate, and the principle of operation is applicable to very thick sensitive volumes. Additional n-type implants, called Deep Depletion Extension (DDE) under the in-pixel p-wells have been added to the manufacturing process in order to eliminate the large parasitic substrate current that would otherwise be present in a normal device. The new design exhibits nearly identical electro-optical performance under reverse bias as the reference PPD pixel it is based on, and the leakage current is effectively suppressed. The characterisation results from both front- and back-side illuminated sensor variants show that the epitaxial layer is fully depleted. This development has the potential to greatly increase the quantum efficiency of PPD CIS at near-infrared and soft X-ray wavelengths.

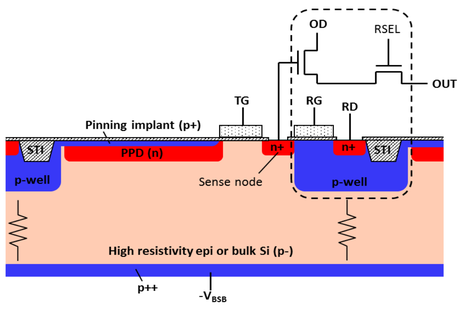
Achieving high QE with PPD pixels



Example of a space-grade CMOS image sensor: CIS115

- To be used in the JANUS visible camera on board ESA's JUICE spacecraft to Jupiter
- 2000(V)×1504(H) 7 µm PPD pixels
- BSI and FSI variants, ≈10 µm thick epi
- Designed by Teledyne e2v

Pinned photodiode is the preferred photosensitive element in CMOS image sensors for science due to their low readout noise, low dark current and high CVF. However, the silicon thickness is usually <10 µm, limiting the QE for near-IR and soft X-rays.

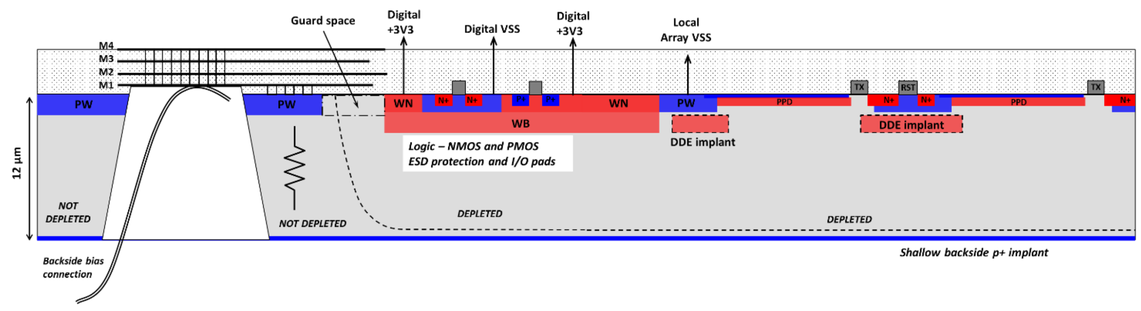


Reverse biasing a PPD pixel is a great way to deplete thick substrate silicon and achieve high QE with minimum MTF deterioration by charge diffusion.

Traditional BSI PPD pixels cannot be reverse biased due to the electrical conduction between the front side p-well and the backside contact via the substrate.

The new design

The new pixel design implements a deep, lightly doped n-type implant under the in-pixel p-wells. This implant, called "deep depletion extension" (DDE) is floating and does not connect to the PPDs.

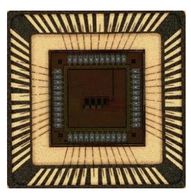


In normal operation the DDE acquires its potential from the adjacent PPDs and becomes depleted. By choosing the appropriate doping profile and size of the DDE, its potential can be made lower than the pinning voltage, but still high enough to create a potential barrier. The DDE region acts as a bridge extending the depletions from the PPDs underneath the p-wells, creating a pinch-off and a potential barrier of sufficient height to prevent undesired substrate currents.

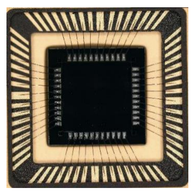
This design has a number of advantages:

- The excellent properties of the PPD are preserved, as it remains unchanged;
- The structure is compatible with any depleted thickness;
- Only one additional manufacturing step is required.

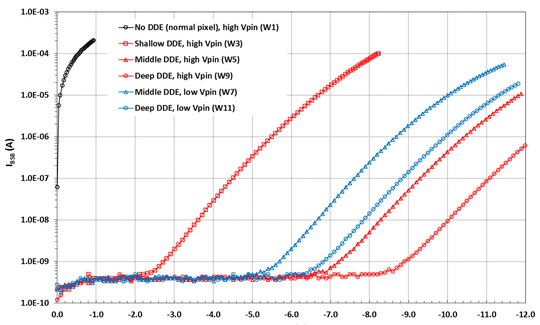
The first prototype

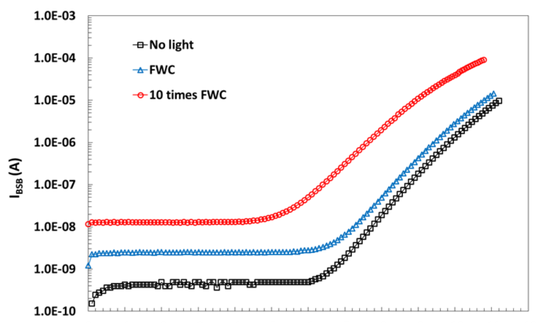


Using 180 nm CIS process from TowerJazz (with modifications) on 18 µm epi for FSI chips; 10 µm and 5.4 µm pixel arrays implemented.



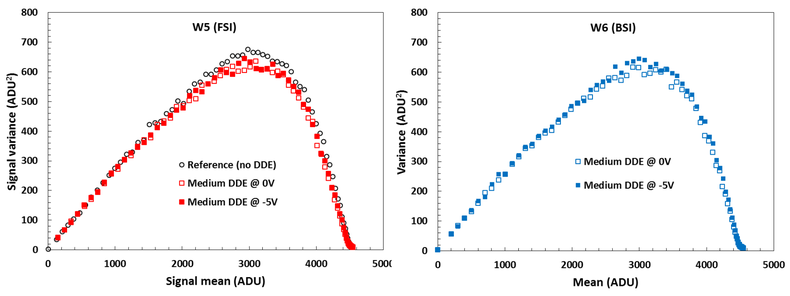
BSI variant (12 µm thick) using proprietary back-thinning process from Teledyne e2v.



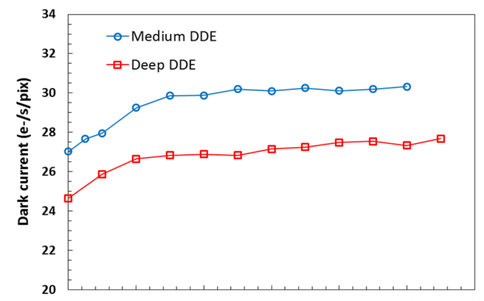


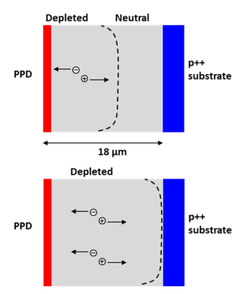
All chip variants can be reverse biased without significant leakage currents, and this is maintained under strong illumination (right). The leakage current mechanism is by thermionic emission of holes over the potential barrier. The onset of this is beyond full depletion, and the voltage threshold depends on the size and depth of the DDE as predicted by TCAD simulations.

The photon transfer curves of the FSI and BSI variants are identical to the reference design.



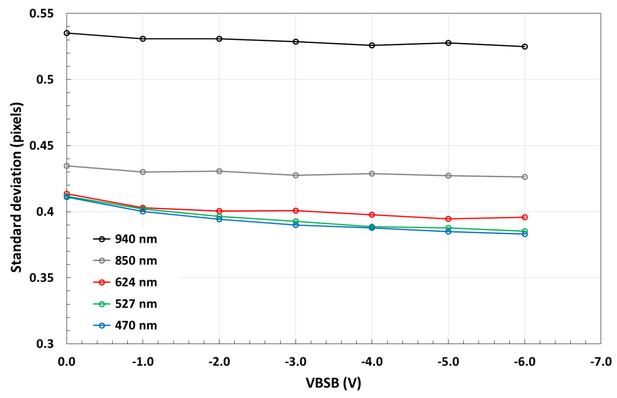
Proving full depletion





As the depletion increases in depth it reaches the backside interface with the p++ substrate and cannot increase anymore; at this point the bulk dark current is expected to level off. In FSI chips the data is consistent with the expectation of full depletion at -4V reverse bias.

Spot pinhole illumination was used to investigate the depletion depth in BSI devices. Short wavelengths (for example 470 nm, 0.6 µm absorption length in silicon) are absorbed near the backside, and if the depletion reaches the back of the device there will be less diffusion. Much longer wavelengths (for example 940 nm, 54 µm absorption length) are absorbed throughout the thickness of the device and the charge spread is much less sensitive to the extent of depletion, in particular in our 12 µm BSI devices.



The spot size dependence on the reverse bias for various wavelengths indicates that the device reaches full depletion.

The QE should be consistent with the silicon thickness.

Reference: Konstantin D. Stefanov, Andrew S. Clarke and Andrew D. Holland, "Fully Depleted Pinned Photodiode CMOS Image Sensor With Reverse Substrate Bias", IEEE Electron Device Letters, Vol. 38, No. 1, pp. 64-66 (2017).

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