High Resolution TDI CMOS Image Sensor Development

23rd June 2021

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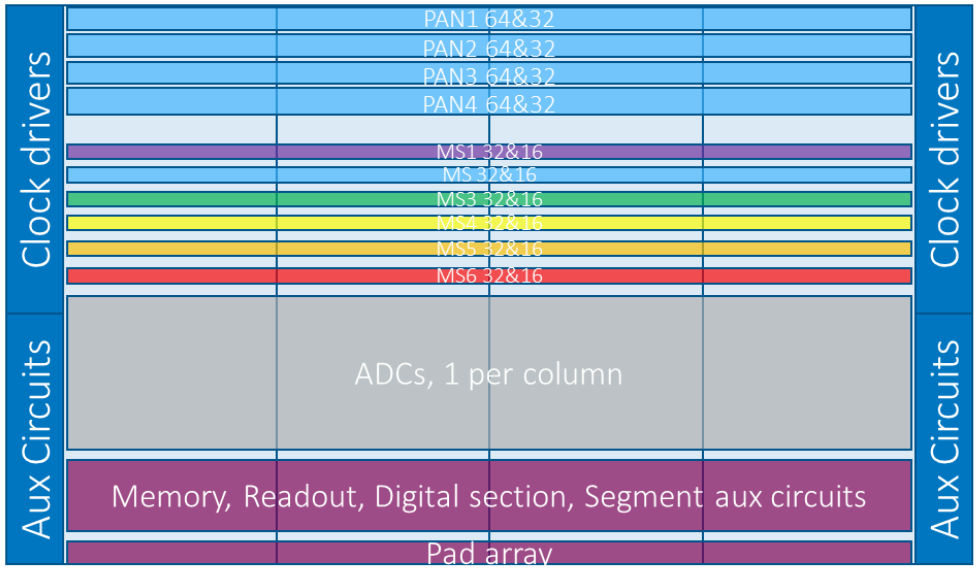
CIS125 – qTDI CMOS

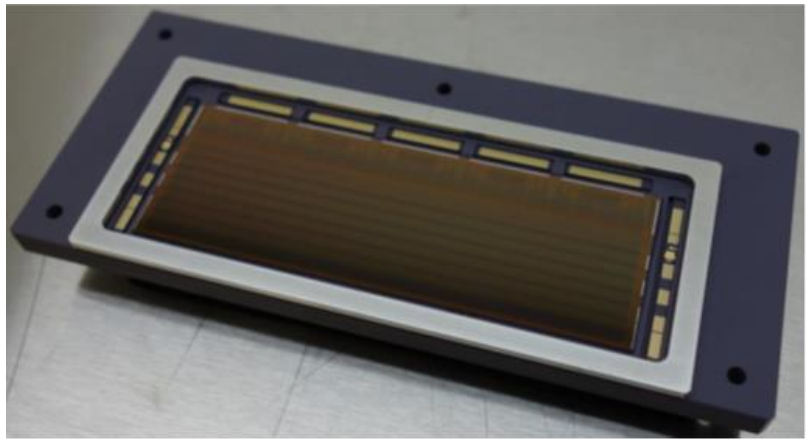
Device Introduction

- In collaboration with CEOI, SSTL and the Open University, Teledyne e2v are developing a high resolution image sensor for applications in Earth Observation.

- Based on a TDI CCD-on-CMOS architecture, the technology takes benefit from the inherent charge transfer benefits of CCD phased electrode pixel structure as well as the highly integrated, low power and in-parallel benefits of CMOS.

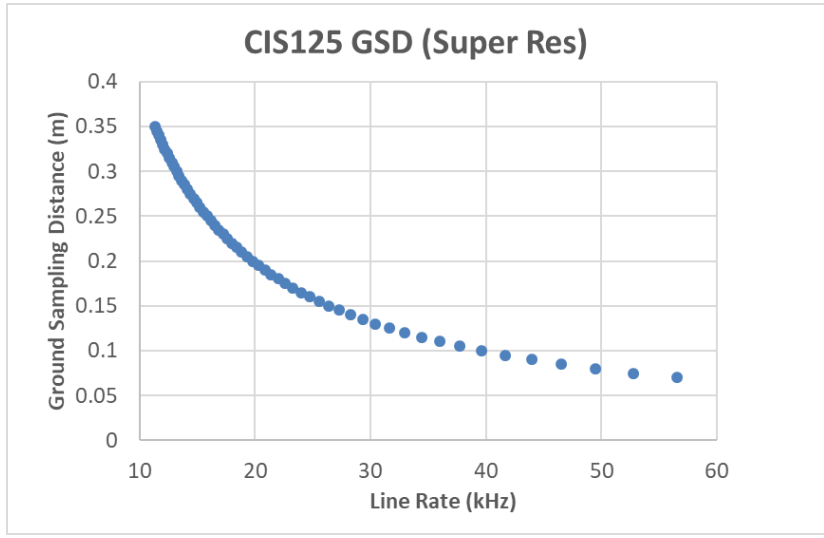
- Key sensor attributes:
  - 4 x 5µm PAN channels (16k columns)
  - 6 x 10µm MS channels (8k columns)
  - PAN half pixel offset (Super res capability)
  - 20 x CML Output at 2.0GBit/s

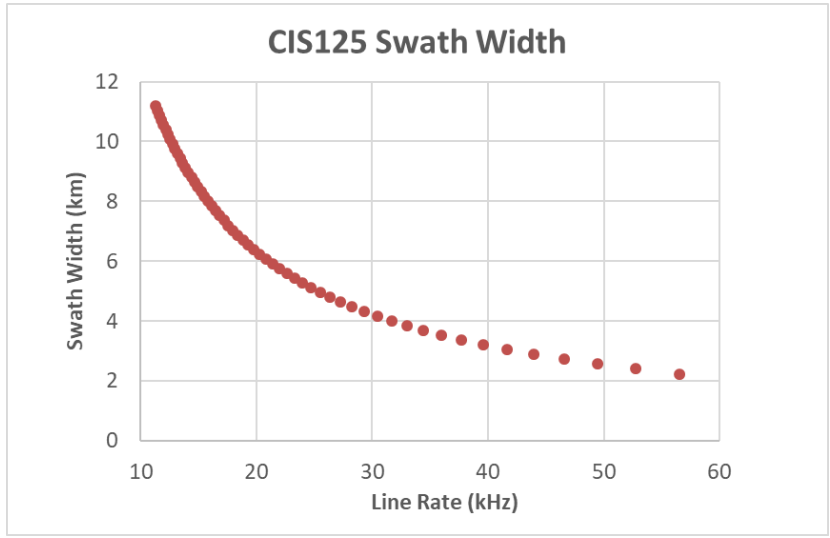




CIS125 Capability and Applications

- The CIS125 is designed to address the new-space market, providing an accessible route to space for both agency and non-agency customers.
- The small (5µm) pixel allows for a very high Ground Sampling Distance (GSD). With super resolution applied, sub 10cm GSD is achievable at detector level.
- The large number of columns (16k PAN) serves to optimise temporal resolution through high swath width.
- 6 x Multispectral channels with potential for customised filters provide a route into a number of surveying applications e.g. monitoring vegetation health, Ice reduction as well as monitoring capability in traffic, mapping, logging jurisdiction, etc.





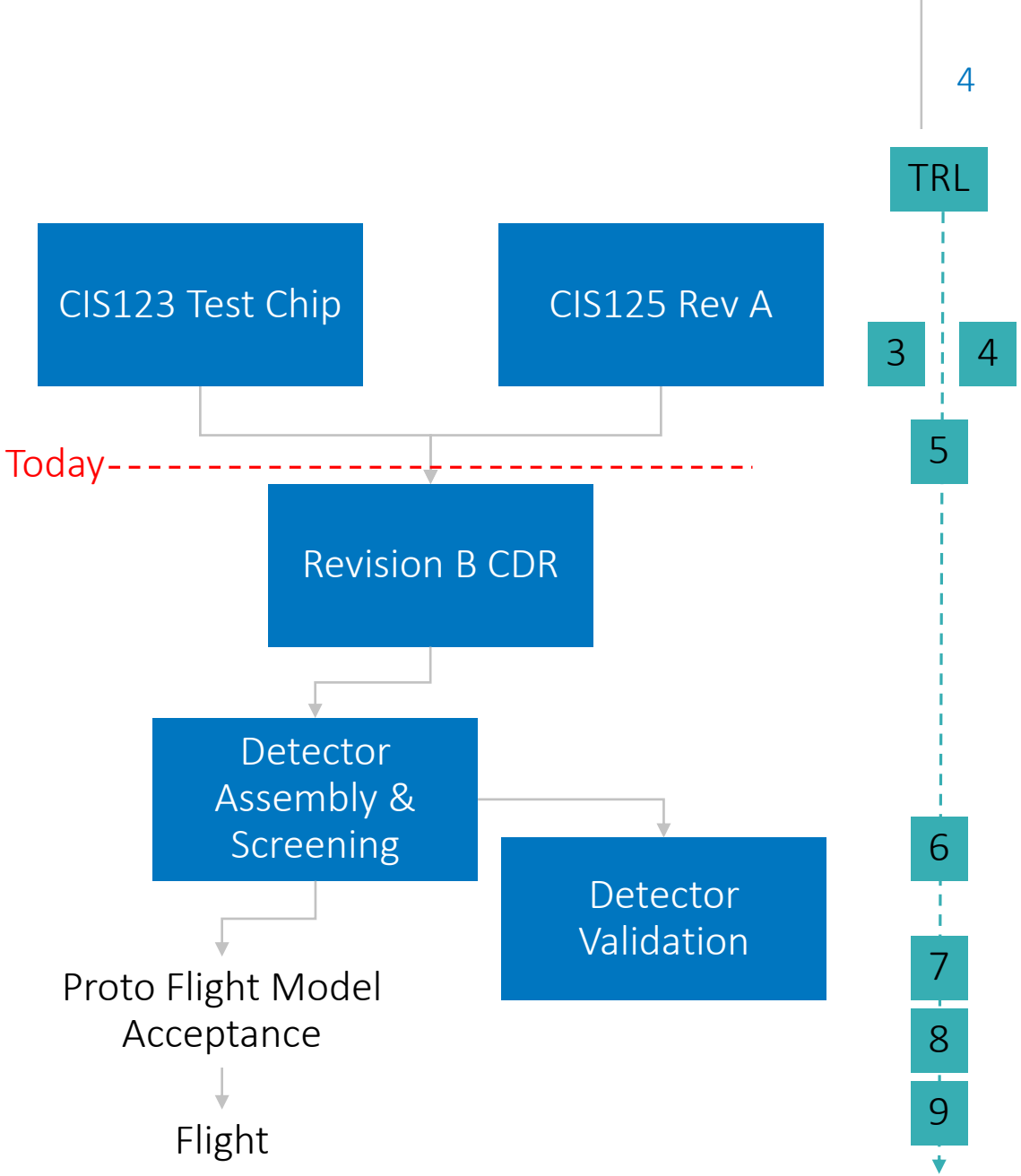
CIS125 Development

- The CIS125 takes significant design heritage from existing Teledyne devices. A key deviation being the choice of foundry which opens up more export accessibility.

- Given the different libraries between foundries (as well as other CIS125 specific design elements), two key elements to be addressed are:

  - Verification of the CCD-on-CMOS pixel capability
    - Assessed via a bespoke analogue test chip – CIS123

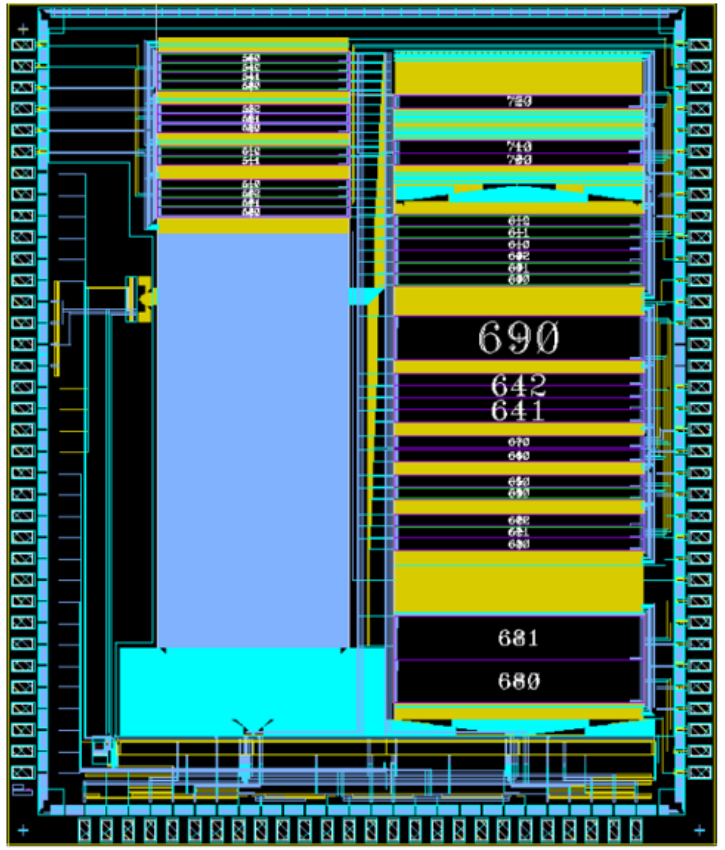
  - Verification of digital periphery elements as ported across foundries
    - Assessed via “revision A” CIS125 devices

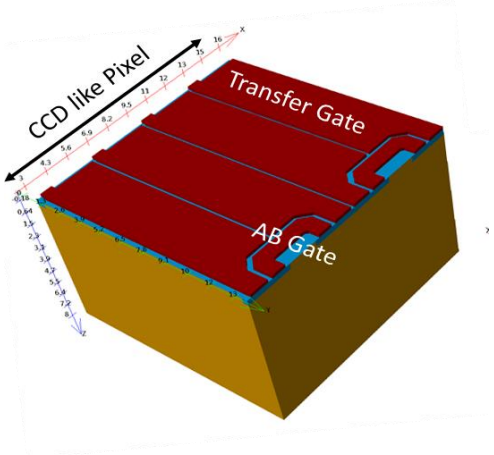


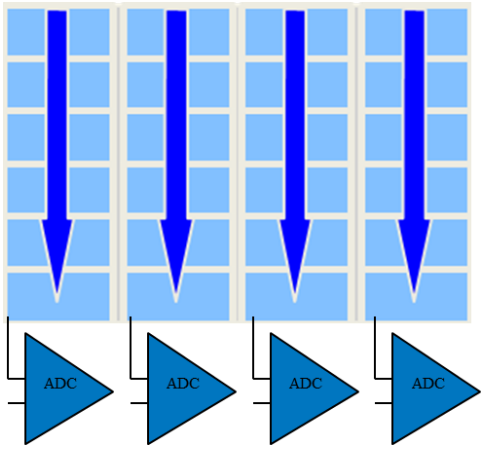
CIS123 – Analogue Test Pixel Vehicle

Device

- The CIS123 is designed to provide information as to the CCD-on-CMOS pixel architecture for a number of variants, across a number of material splits.
- The optimised pixel output will then be implemented into the future revision of the CIS125.
- The pixel/split variations include:
  - Pixel sizes: 5µm, 6.5µm and 7µm
  - Varying antiblooming architectures
  - Alternative sense node architectures for noise optimisation
  - Different channel dose and energy conditions to optimise full well capacity



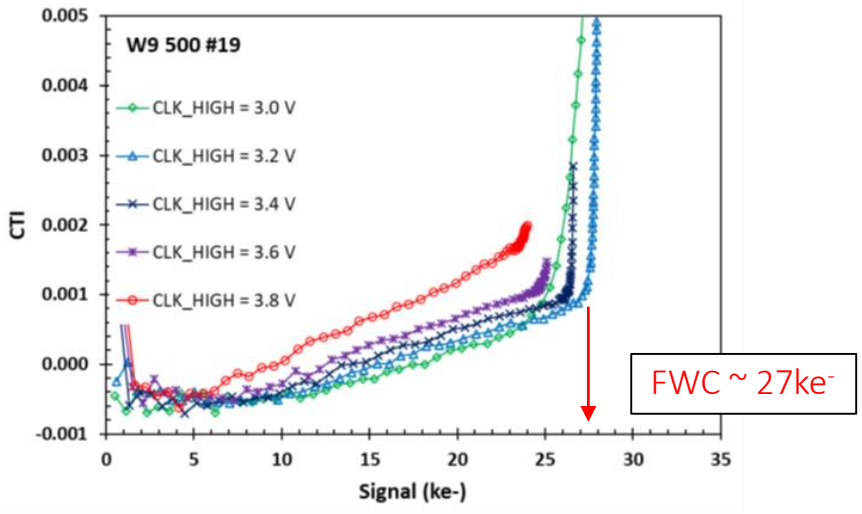




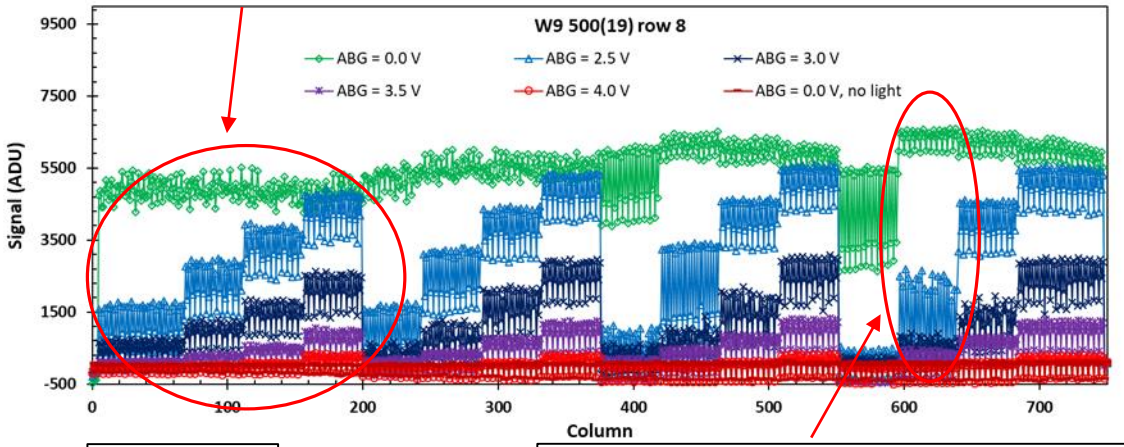
CIS123 – Analogue Test

Results

- Key parameters to be investigated through the analogue test chip are:
  - Full Well Capacity (as limited by charge transfer degradation)
    - i.e. how well can charge transfer across non-overlapping poly gaps?
  - Antiblooming functionality
    - i.e. can the pixel architecture handle significant oversaturation without blooming?
  - Pixel Linearity
  - Dark Signal



4 x 4 antiblooming architectures on a single image array



~15x FWC

Highest capacity architecture identified

CIS123

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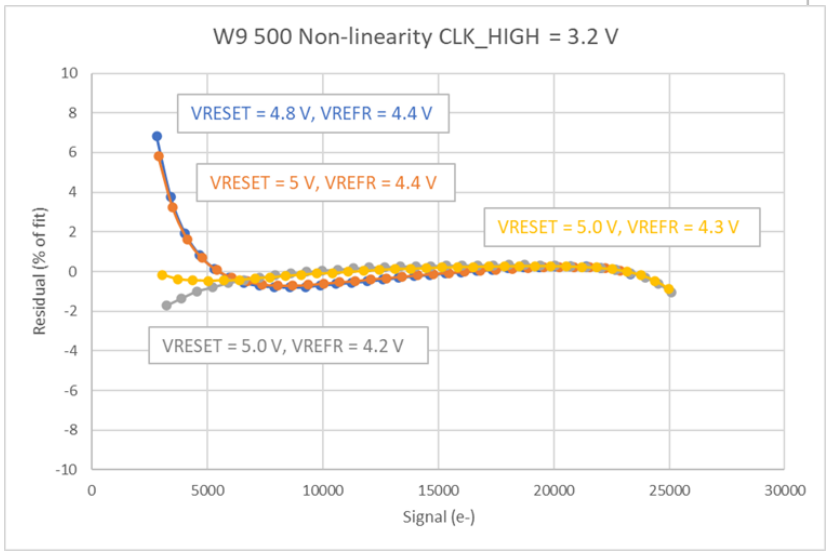
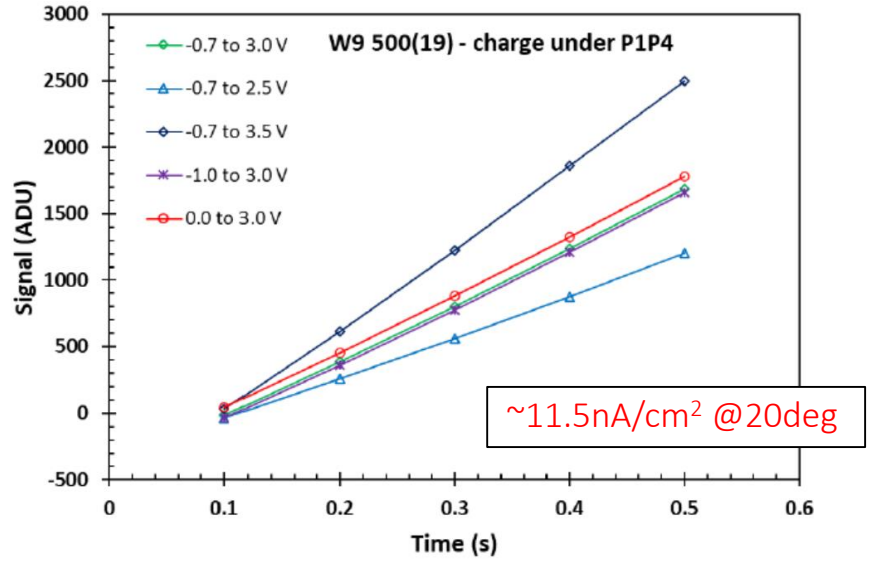
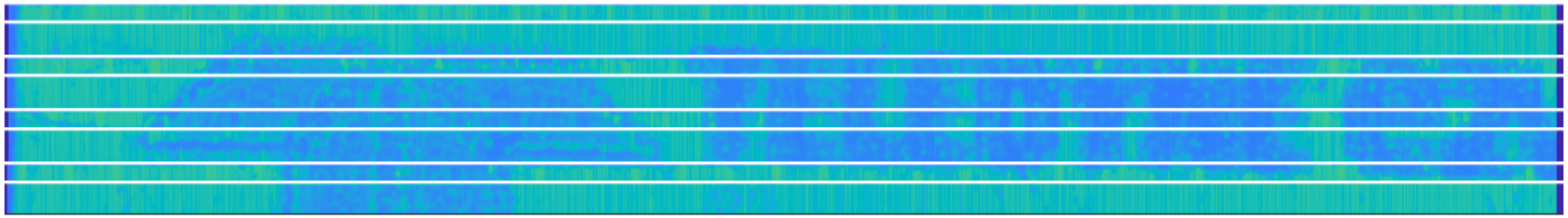




CIS125 - Digital Assessment

- In parallel with CIS123 assessment, CIS125 has been functionally characterised at Teledyne e2v.
- Overall SPI, biasing, supplies and synchronisation of segments is working as expected.
- Digital cores are working at full speed
- ADC is functional and converting inputs into meaningful code..
- Perhiphery and imaging section are communicating well and are synchronous.
- The full chain pixel, ADC, digital core, serialiser, CML and board communicate as expected.



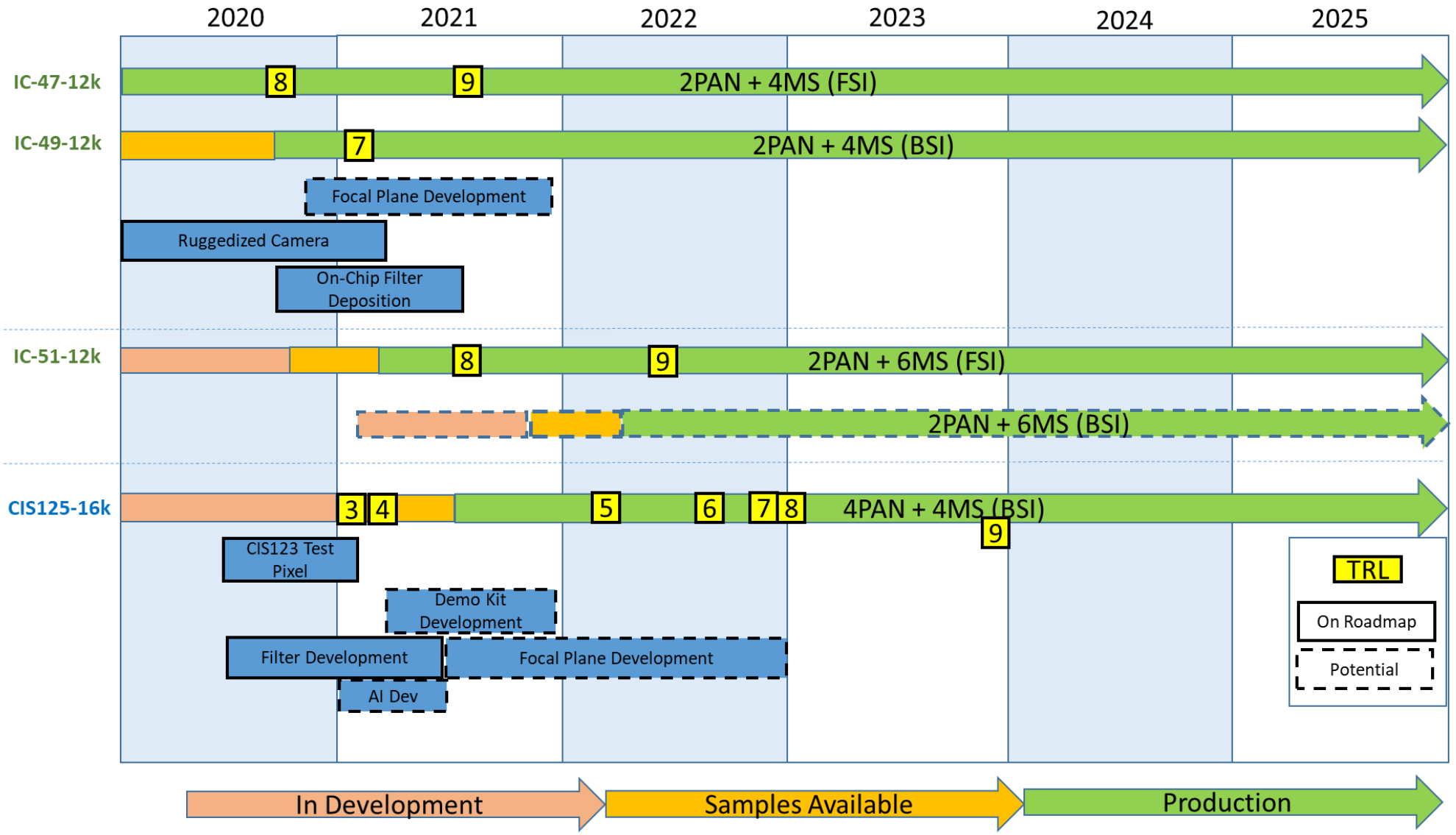
Power Consumption <9.5W

CIS125 – Digital Assessment

Next Steps

- Finalise Debugging as input to Rev B CDR
- Additional characterisation of the ADC (optimisation of Noise and timing profiles)
- TDI Testing (using an older pixel design)
  - Charge Injection
  - Bi-Directionality
  - Fixed Pattern Noise
- Alternative operating modes

Orbis Roadmap



Auxiliary Activity

AI Imaging Processing Algorithms

- The high speed digital outputs and pixel count associated with the CIS125 generates significant volumes of data.
- Data management creates significant system level complexity in satellites and downlinking.
- Working with CRAFT Prospect, advances have been made in concepts for AI processing algorithms.
  - ID useful imagery
  - Real-time object detection to speed in intervention
- Demonstration platform established to simulate CIS125 data with applied image processing