Industrial Research for Next-Generation Radar Electronics

Project Review Day

10th December 2018

Matt O'Donnell on behalf of Mike Gibbons

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Agenda

- Overview / Objectives
- Sentinel-1 ICE RxM Adaptation
- NIA Computer Integration
- Xilinx V5 Mounting Qualification

Overview / Objectives

- This CEOI-ST Flagship project objective was to make enhancements to existing Radar Electronics products developed by Airbus Defence and Space in Portsmouth to enable them to support a broader range of future missions.
  - The research and critical developments to be undertaken would include the evolution and demonstration of hardware modules applicable to the Integrated Central Electronics (ICE), originally developed for Sentinel-1, and to the New Instrument Architecture (NIA), based on the product developed for NovaSAR-S.
  - The requirements of the BIOMASS and the SAOCOM-CS missions (to the extent that they were known at the beginning of the project) would be used to guide the bread-boarding and demonstration activities.
- The work was broken down into three areas:
  - Sentinel-1 ICE Receive Module modification & bread-boarding for low frequency operation and enhanced science data interface flexibility
  - Development of an embedded computer option for the NIA product to broaden its applicability to a range of future ESA missions.
  - Qualification of the Virtex-5 FPGA used in NIA in agreement with ESA parts experts

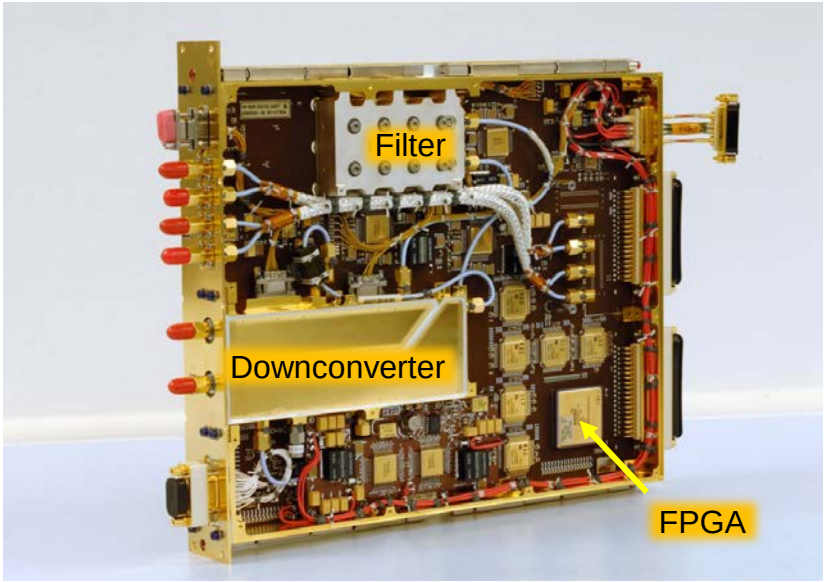
Highlights Summary

- Project metrics
  - Duration: 3 years (KO 19/3/2015 – Final Report 4/3/2018)
  - Cost: £1.6M from R&D + CEOI 50/50 co-funded
- Barriers
  - Agreement between Xilinx and ESA on the NDA permitting release of part qualification
  - Xilinx FPGA test code development engineer left before completing the code
  - Problems with the V5 qualification PCB during months of thermal cycling resulting in delays, investigation and re-test
  - Manufacturing fault on the RxM stopped full verification of the assembly
- Breakthroughs
  - Agreement with ESA on the V5 qualification plan
  - Successful completion of the V5 qual. in spite of the problems encountered
- Outcomes & Aftermath
  - Sentinel-1 ICE RxM adaptability confirmed and design ready for P-band (e.g. BIOMASS)
  - Integration of computer function with NIA has been demonstrated
  - NIA qualification of the V5 clamped mounting and acceptance of Xilinx part qualification positions the hardware for future ESA programmes – a potential back-up for Copernicus ROSE-L mission (under certain operational constraints)

Sentinel-1 ICE RxM Adaptation

- The purpose of this breadboard development is to place the ICE design in a low risk position for the anticipated BIOMASS program by validation of the functional changes to the RxM.
- The P-Band Receive Module requirements are derived from the Sentinel-1 Receive Module requirements and have been modified to take account of:
  - The Frequency Plan for P-Band (435 MHz)
  - Output of SAR data packets using SpaceWire
- This work is split into 4 principal activities as follows:
  - P-Band Filter
  - P-Band Downconverter
  - Control & Interface FPGA (CIF) Enhancement
  - RxM PCB modification, RxM build and test

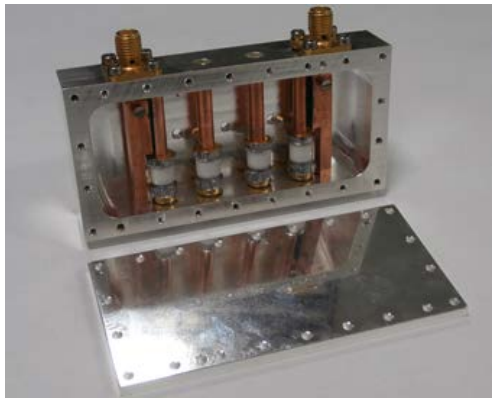
Sentinel-1 Receive Module (RxM)

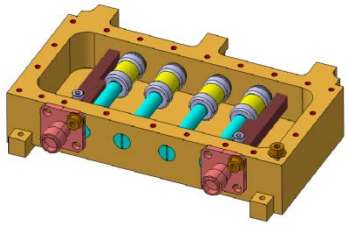


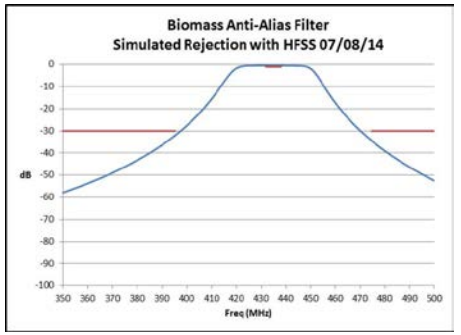
Sentinel-1 ICE RxM Adaptation

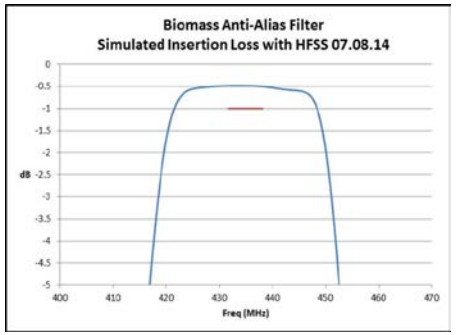
➢ P-Band Filter

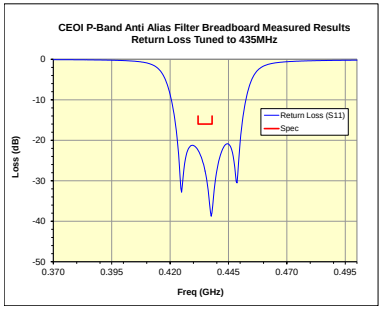
- Primary function is to block the Image channel from conversion into the IF channel
- Main concern was about maintaining the performance and physical dimensions at x12 lower frequency
- Cavity Combline filter technology has been chosen with cavity size of 12mm ensuring the filter fits with the volume available. HFSS modelling demonstrated good performance...
- CAD model and physical realisation of the filter shown below
- Results achieved compliant to requirements

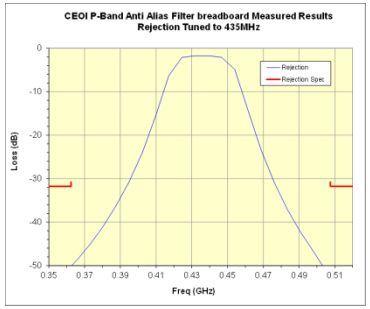


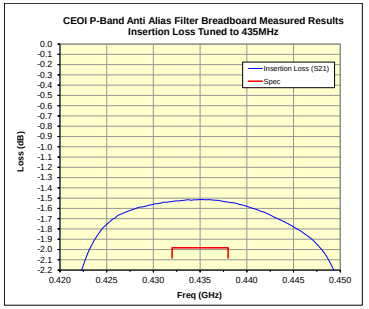












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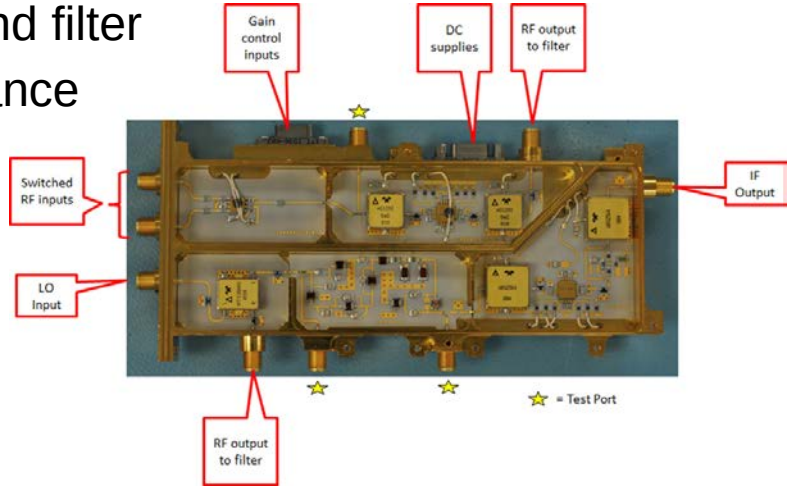
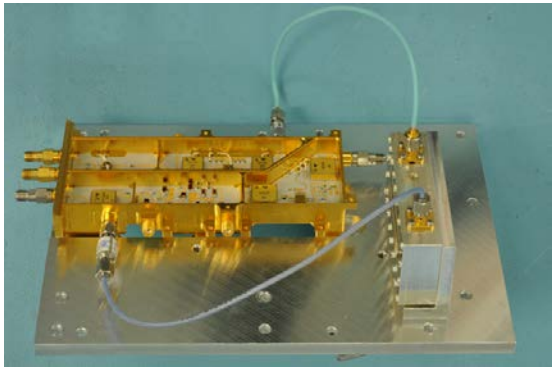
Sentinel-1 ICE RxM Adaptation

➢ P-Band Downconverter

- One of the most significant changes from the heritage Sentinel-1 product is the frequency plan. The heritage design uses a frequency plan for a C-Band mission at 5405 MHz, whereas the target BIOMASS mission has a P-band centre frequency of 435MHz.
- A frequency plan trade-off was performed to select the optimum configuration for P-Band and maintain fully synchronous frequencies from the Ultra Stable Oscillator (USO). Constraints from the ADC and ASIC parts in the Sentinel-1 design had to be considered
- Although direct digital sampling of the P-band signal is possible the chosen frequency plan uses a single RF conversion in both the transmit and receive paths, which follows the heritage architecture and reduces the risk of timing problems in the digital electronics.
- An EM quality Downconverter has been designed and built and has been tested in conjunction with the P-Band filter with no major non-compliance

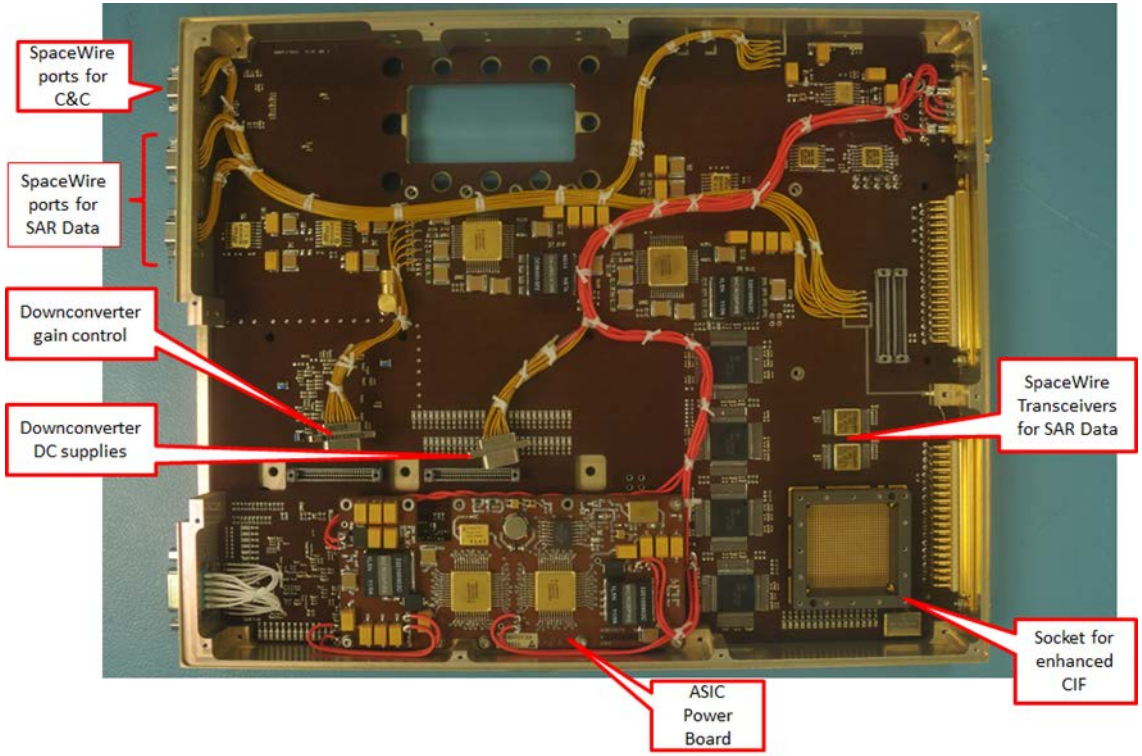




Sentinel-1 ICE RxM Adaptation

➢ Control & Interface FPGA (CIF) Enhancement

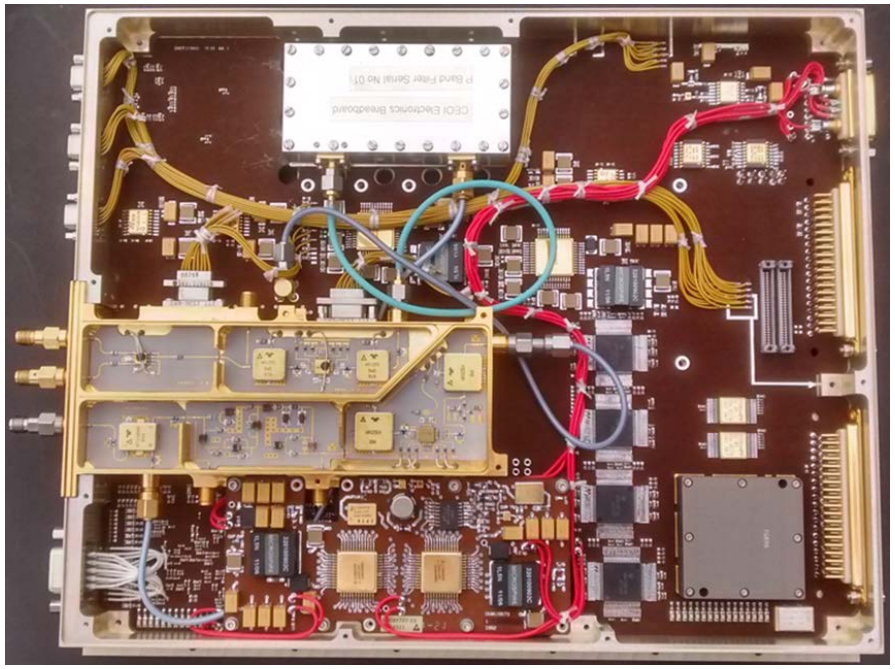
- The Control and Interfaces FPGA has been enhanced to support narrow band missions such as BIOMASS where the required bandwidth and resultant SAR data rate is sufficiently low for SAR data to be streamed over a single SpaceWire channel
- The key CIF enhancement is provision of prime and redundant SpaceWire interfaces for SAR data rather than high rate WizardLink interfaces as required by Sentinel-1
- FIFO buffers not needed for low rate data have been replaced by Spacewire transceivers on the board
- FPGA coded and debugged successfully using developer tools
- PCB design adapted to suit changes to the interface

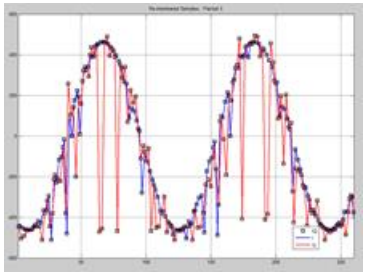


Sentinel-1 ICE RxM Adaptation

➢ End-to-End Testing

- A complete adapted RxM was manufactured and assembled with the new P-band filter, Downconverter and CIF interfaces
- An analogue sinusoid representing a radar Rx signal was introduced to verify the throughput signal integrity
- A board manufacturing problem was found causing poor signals from one of the ASICs to the CIF, a ‘dry’ joint on one of the ASIC solder bumps was suspected.
- A work-around was introduced to get the best results possible without major re-work to the board; good confidence in the design has been achieved with this technique





Re-constructed Sinusoid with faulty ASIC contact

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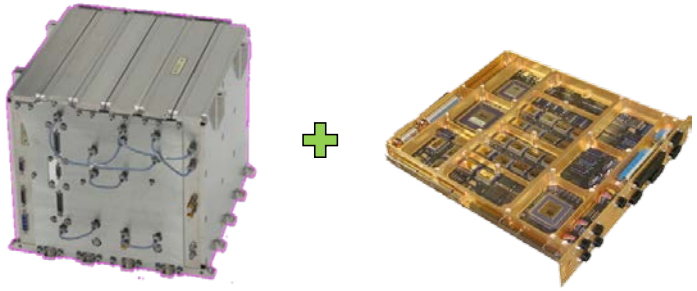
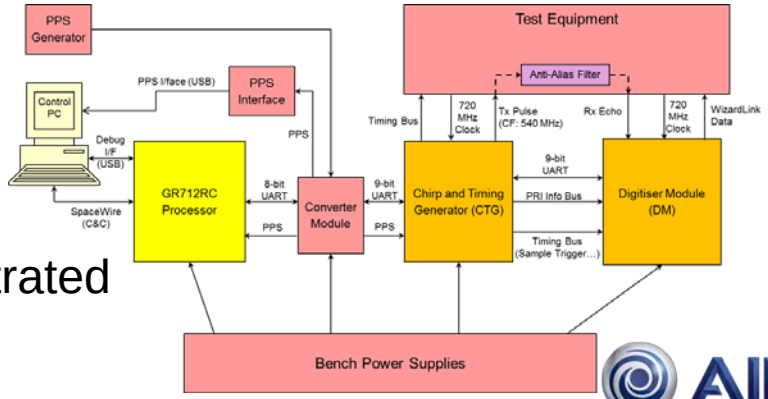
NIA Computer Integration



NIA Radar Electronics
(NovaSAR-S Hardware)
+ ICU Concept

➢ NIA

- NIA (New Instrument Architecture) is a flexible Synthetic Aperture Radar (SAR) instrument architecture developed by Airbus Defence and Space Ltd., using reprogrammable Virtex-5 FPGAs and targeted at low-cost missions.
- To save cost the command and control functions are performed by the Platform computer, however ESA missions typically require autonomous Instrument operations so addition of an Instrument Control Unit (ICU) has been undertaken
- Following an analysis of the requirements an implementation trade-off was carried out and a LEON3 processor was selected
- A development processor board was procured and assembled in a development test environment with the NIA hardware; a DM CTG (Chirp and Timing Generator) was manufactured to complement the Digitiser DM already available.
- Software was developed to simulate the OBC, and processor code developed to control the NIA hardware
- The principles and practise of implementing the ICU functions in NIA have been demonstrated



Test Configuration

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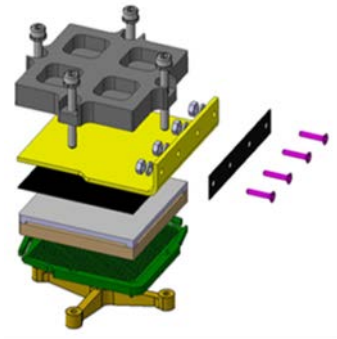
Xilinx V5 Mounting Qualification

➢ Outline

- The plan was to complete the assembly qualification for a Xilinx Virtex 5 FPGA component assembled to a Polyimide PCB using a clamped cin::apse ‘fuzz button’ connector; ESA were to be involved.
- ESA were given access to data from the part qualification undertaken by the manufacturer.
- For the mounting qualification a total of 9 packaged devices were subjected to environmental conditions agreed in a detailed plan, of which 3 were active and monitored electrically throughout the thermal cycling.
  - Ground storage simulation
  - Vibration & Shock
  - Thermal Vacuum & Thermal cycling (1500 cycles)
- The parts have survived all tests with no electrical defects
- DPA has been carried-out and no faults observed
- Qualification is therefore successful!
- Problems to be overcome during the thermal cycling included:
  - Moisture damage to PCB during thermal cycling
  - Failure of test some test PCB parts toward the end of testing



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