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THE DESIGN AND DEVELOPMENT OF LOW- AND HIGH-VOLTAGE ASICS FOR SPACE-BORNE CCD CAMERAS

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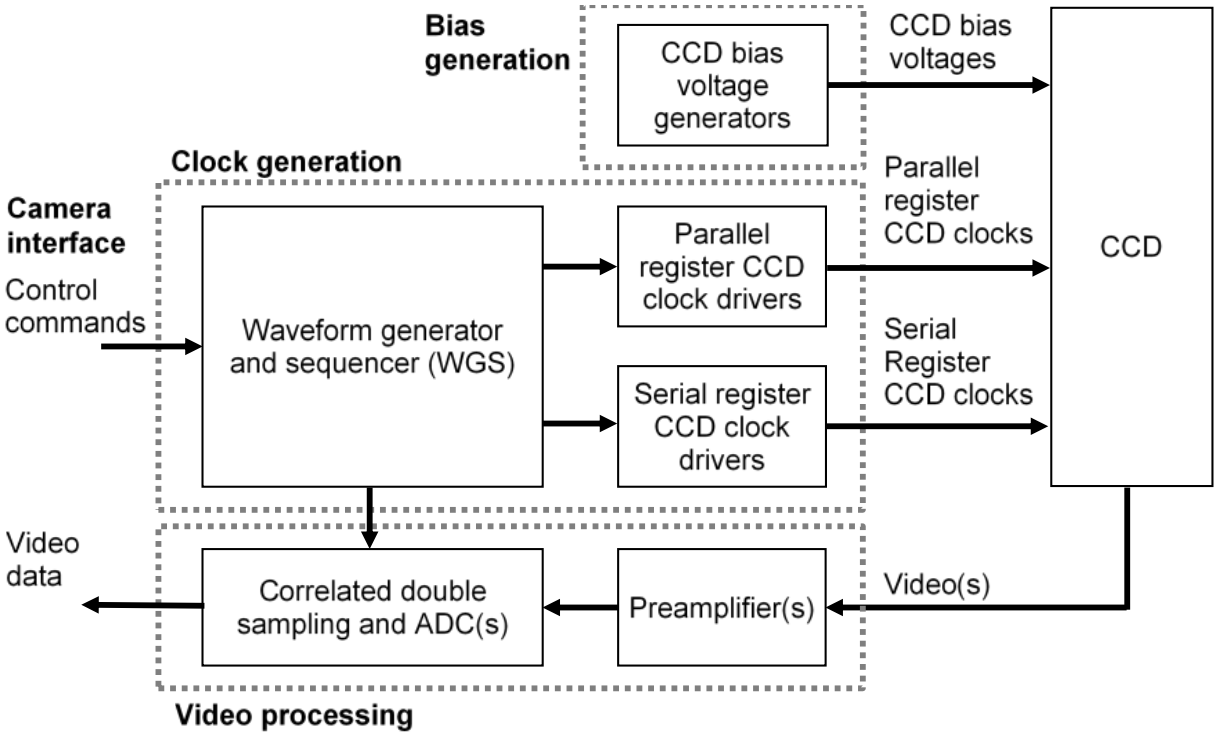
RAL Space

Contents

CCD camera readout electronics system



Control logic: Generate all timing signals

- **Typically implemented in a radiation-tolerant FPGA**

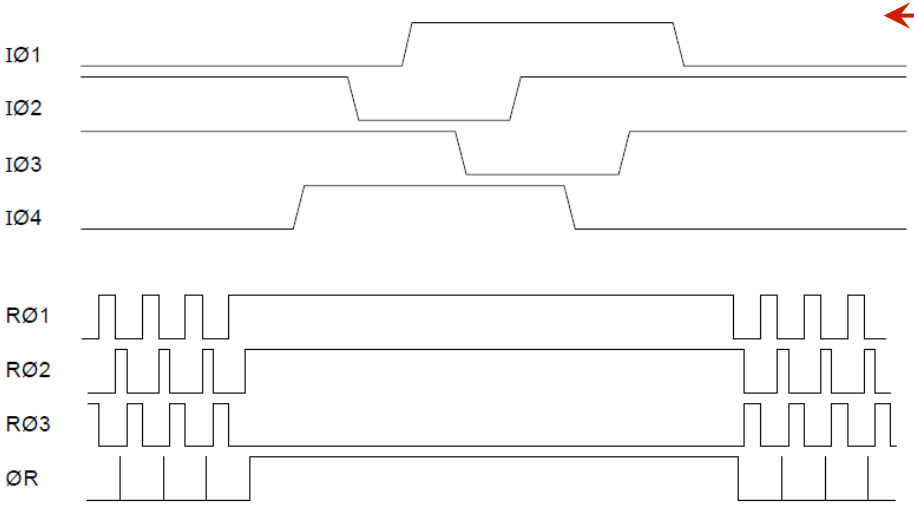
Multiple-phase CCD clock drivers to clock the signal charge to charge detection amplifiers

Low-noise DC bias supplies to operate the CCD's output amplifier(s) and charge drains

One or more video preamplifiers, CDS signal processors and analogue-to-digital converters

Typical CCD clock waveforms

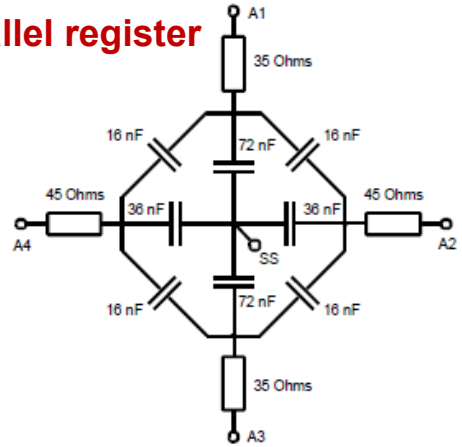
Parallel clocks



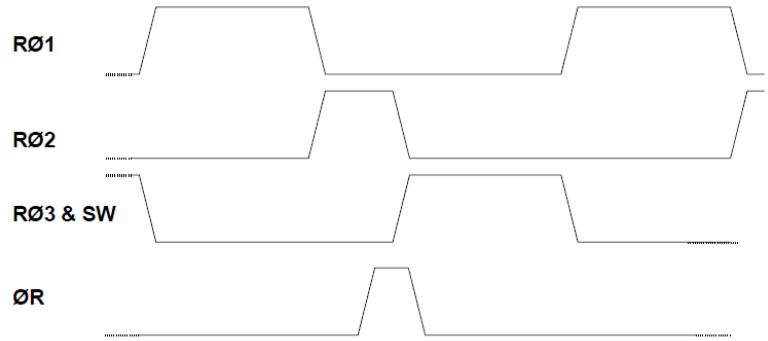
Amplitude ~ 10 V

Frequency ~ 10-100 kHz

4k x 2k pixel parallel register
Typical loading



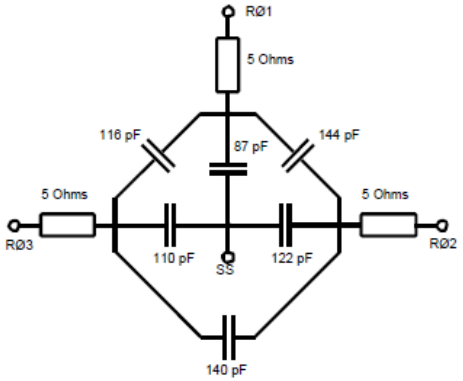
Serial clocks



Amplitude ~ 10 V

Frequency ~ 0.1-2 MHz

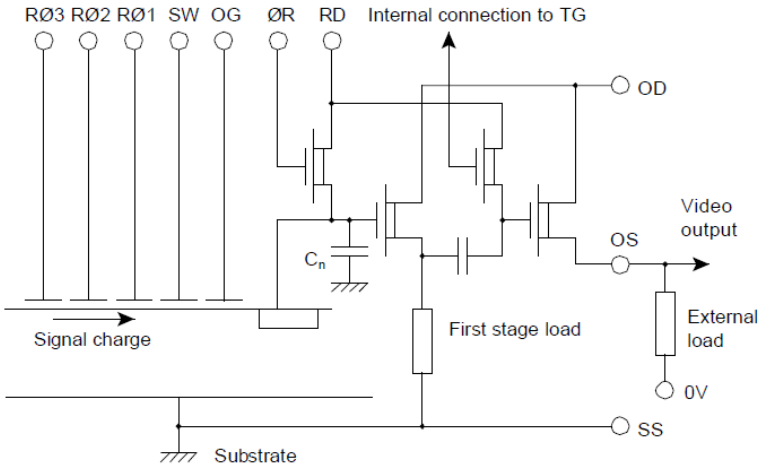
4k pixel serial register
Typical loading



Clock drivers must translate logic-level signals to ~ 10 V amplitude analogue waveforms with sufficient current drive for the CCD's capacitive electrode

Output amplifier bias and video output

Charge detection amplifier

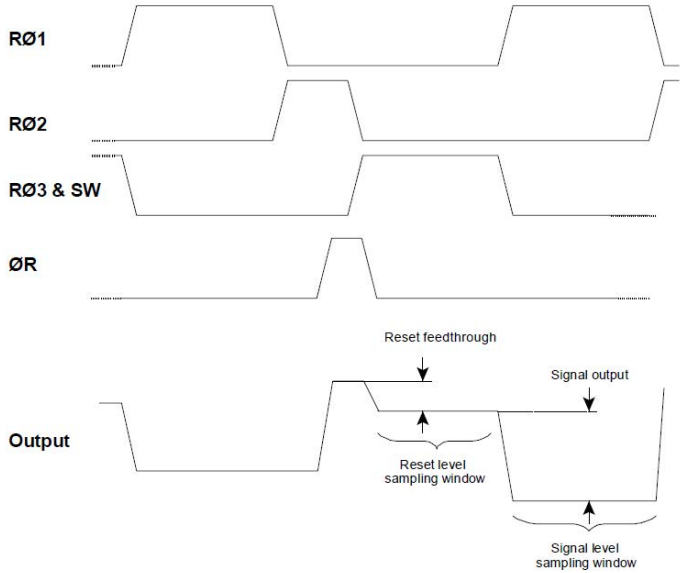


Charge detection amplifier requires several low-noise DC bias voltages

Output Drain (OD) Bias: ~ 30 V

Reset Drain (RD) Bias: ~ 17 V

Video output waveform



Video output signal swing ~ 1 V

Correlated Double Sampling (CDS)

Signal output = Signal level – Reference level

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Camera electronics design challenges

System requirements

- Low-volume, low-mass, low-power
- High-reliability and space-qualified components
- Sufficient tolerance to the effects of space radiation

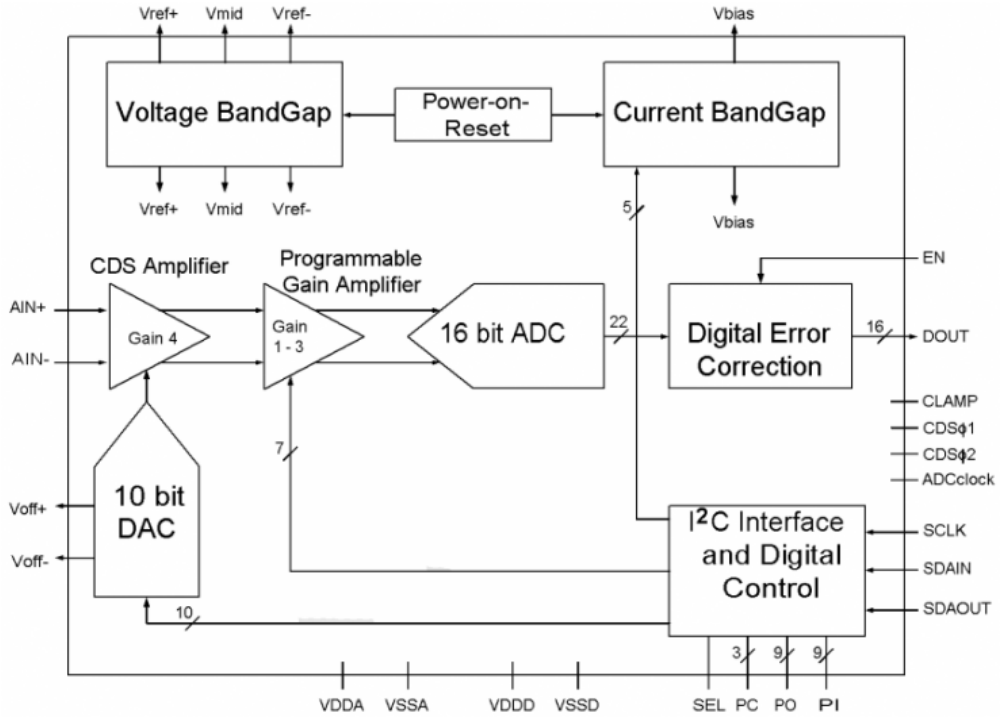
Electronic component challenges

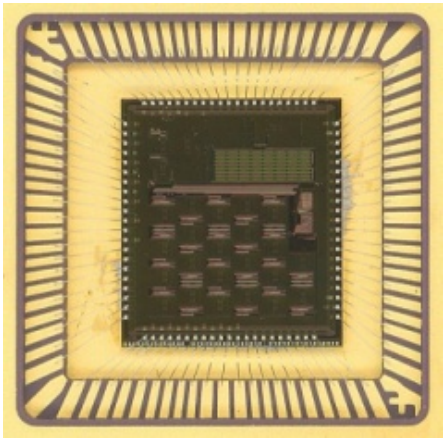
- Space-qualified components acceptable to international space agencies (ESA/NASA) are frequently unavailable
- Up-screened commercial components may not meet project requirements

Our approach at the STFC Rutherford Appleton Laboratory

- Design and space-qualification of low- and high-voltage mixed-signal ASICs

CCD video processing ASIC



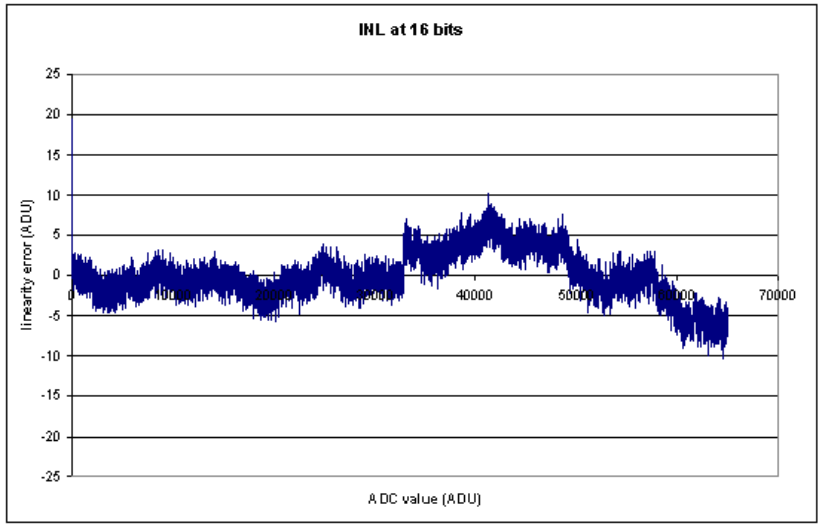


Features

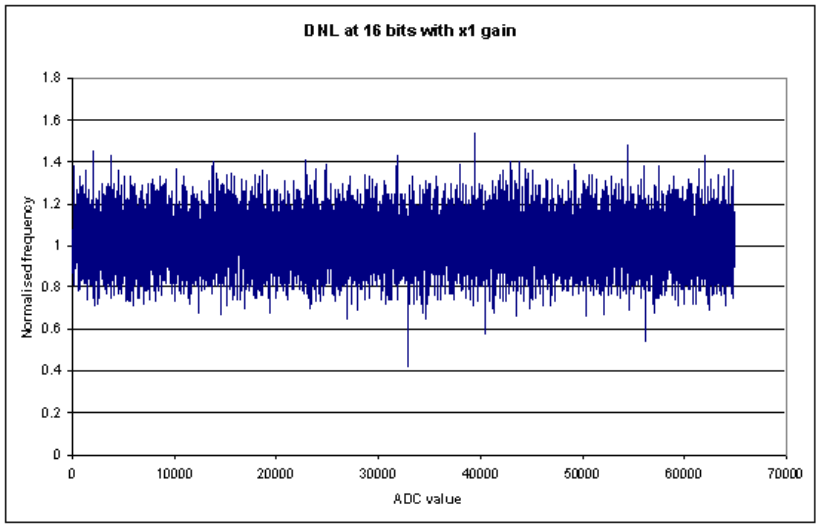
- DC Restoration of the CCD video signal
- Fully differential-input preamplifier and CDS
- 1 V video signal input range
- Fully differential pipelined 16 bit ADC with digital error correction
- Operation at up to at 2 Mpixels/s
- 10 bit Programmable Offset (+/- 500 mV)
- 7 bit Programmable Gain (gain = x 1 to x 3)
- Input referred system noise: 3 adu rms
- TMR protection against single-event upsets
- Power dissipation ~ 400 mW
- AMS C35 0.35 μm CMOS process

CCD video processing ASIC

Integral non-linearity (INL)



Differential non-linearity (DNL)



Performance

Video signal input range	= 1 V
Digitisation	= 16 bits
Operation	≤ 2 Mpixels/s
Input referred noise	= 3 adu rms
	= 46 μV rms
e2v CCD203 (4.5 μV/ e^-)	= 10.2 e^- rms
Integral non-linearity	~ ±10 LSBs
Differential non-linearity	~ ±0.3 LSBs
Power dissipation	~ 400 mW

Radiation test results

Total ionising dose (TID)	≥ 50 krad(Si)
SEL LET threshold	~ 14 MeVcm^{2}mg^{-1}

SEL linear energy transfer profile (LET) examined to 34 MeVcm^{2}mg^{-1} at Cyclotron Facility of Louvain-la-Neuve in Belgium using Ne^{4+}, Ar^{8+} and Kr^{17+} ions

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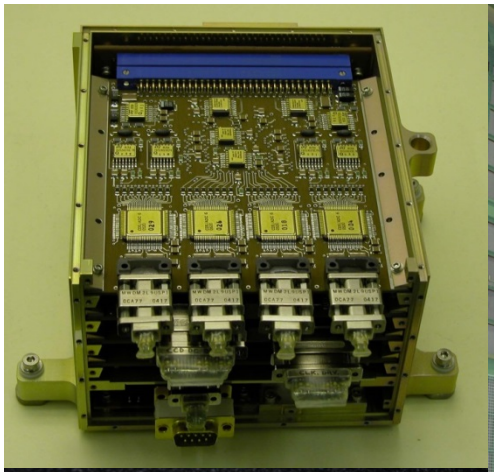
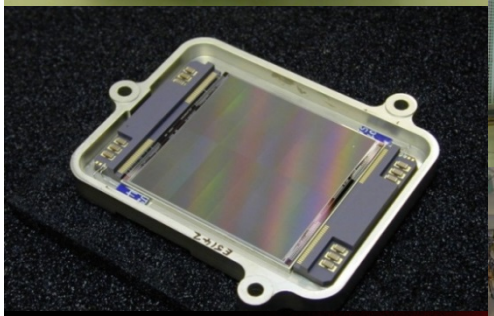
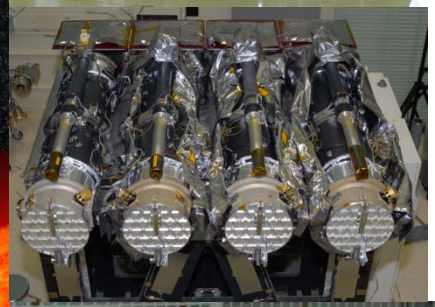
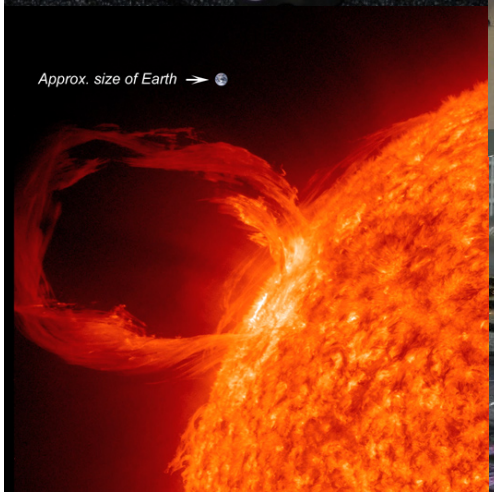
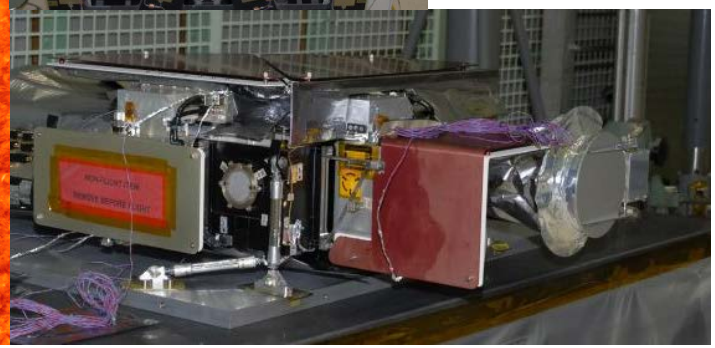
Solar Dynamic Observatory











NASA's Flagship Solar Mission

Launched 11 Feb 2010

Atmospheric Imaging Assembly (AIA)

Helioseismic and Magnetic Imager (HMI)

Custom-designed e2v CCD203

4k × 4k pixels and 12 µm pixel pitch

4-port readout at 2 Mpixels/s each

SEL LET threshold ~ 14 MeVcm^{2}mg^{-1}

Video ASICs individually protected with current-sense / current-trip circuitry

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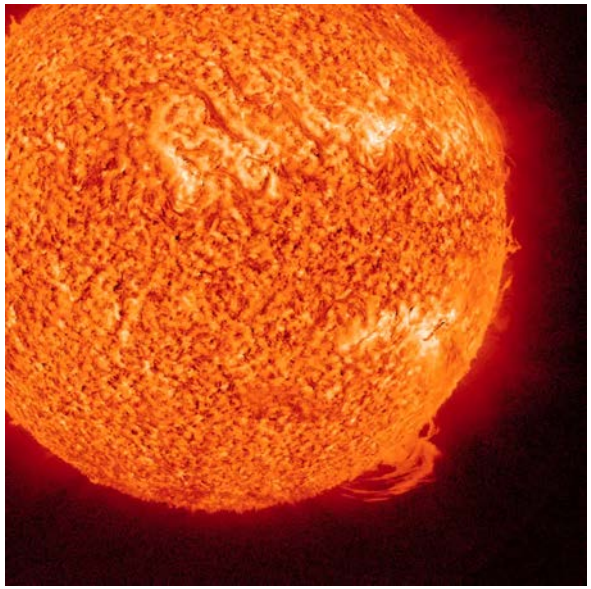
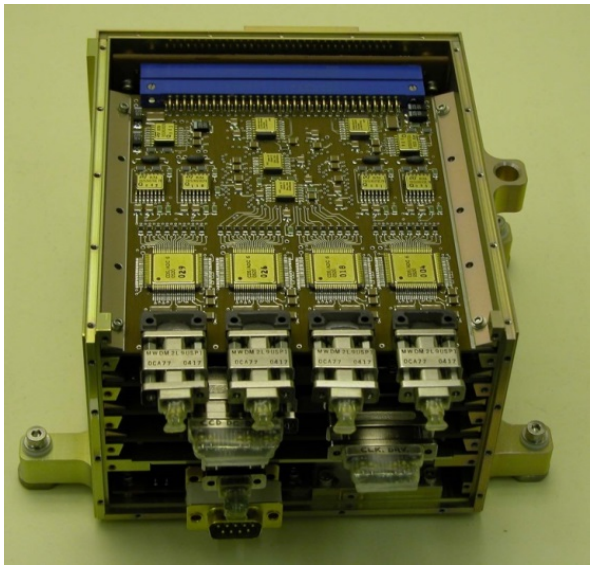


Progress along a Technology Roadmap

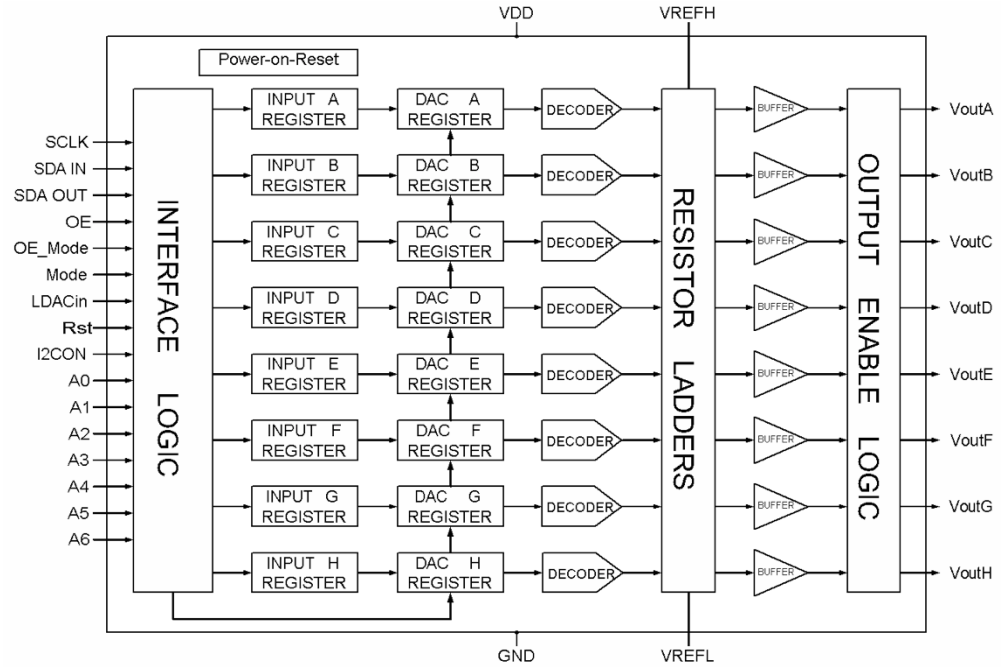
- Have demonstrated Low-voltage CCD ASIC technology
- But susceptibility to Single-Event Latchup remains

Where next?

- Radiation-hardening against SEL
- Greater functional integration
  - ➢ High-voltage CCD ASICs



Low-voltage DAC ASIC



Features

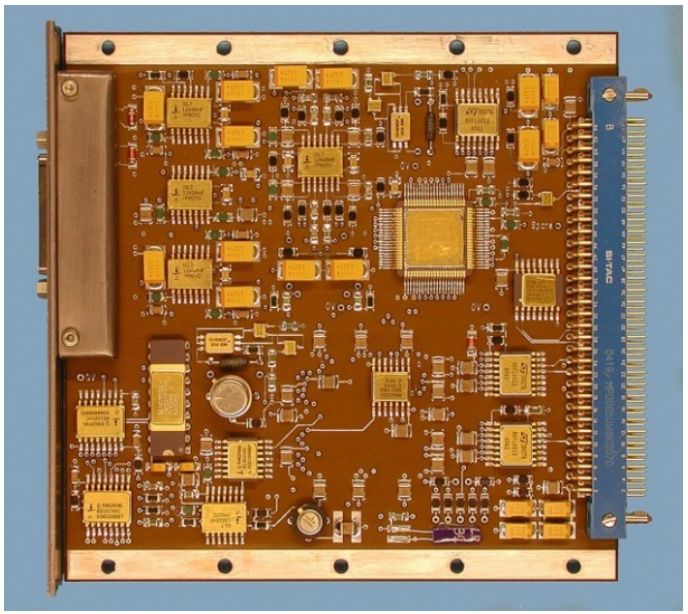
8-channel 10-bit voltage output DACs

Voltage output: 0-2.5 V

Supply: 3.3 V

AMS C35 0.35 μm CMOS process

SEL LET threshold ~ 20 MeVcm^{2}mg^{-1}



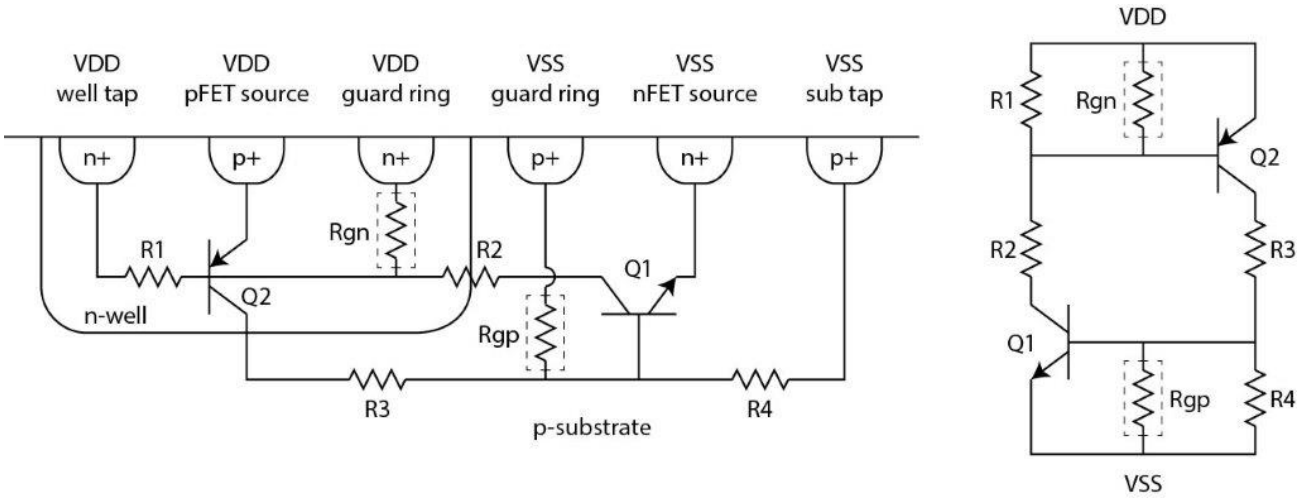
Flown on NASA's SDO

DAC protected with current-sense and current-trip circuitry

Guard-Ring Technology

Latchup

- Latchup is the creation of a low impedance path between the power supply rails
- Latchup is caused by the triggering of parasitic bipolar structures within an IC, in the case of the Space environment, by an energetic particle
- Implanted guard-rings of low-impedance can prevent SEL



Mk 3 Low-voltage DAC Radiation test results

- No SEL events
- SEL LET threshold ≥ 130 MeVcm^{2}mg^{-1} Effectively SEL immune

High-voltage ASICs

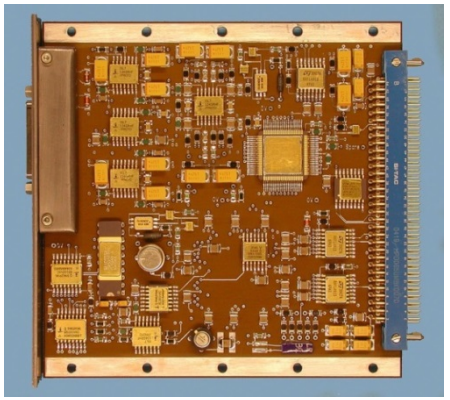
SDO bias card

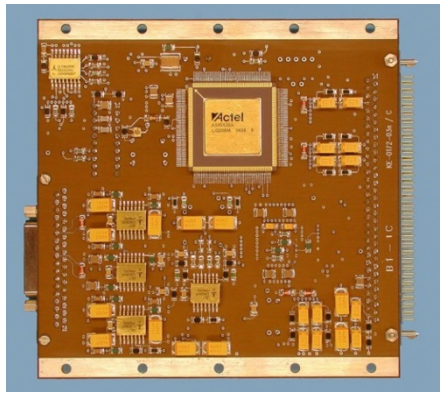
120 mm x 120 mm PCB

7 CCD bias voltages set by a DAC ASIC

16-channel housekeeping telemetry

Something better??





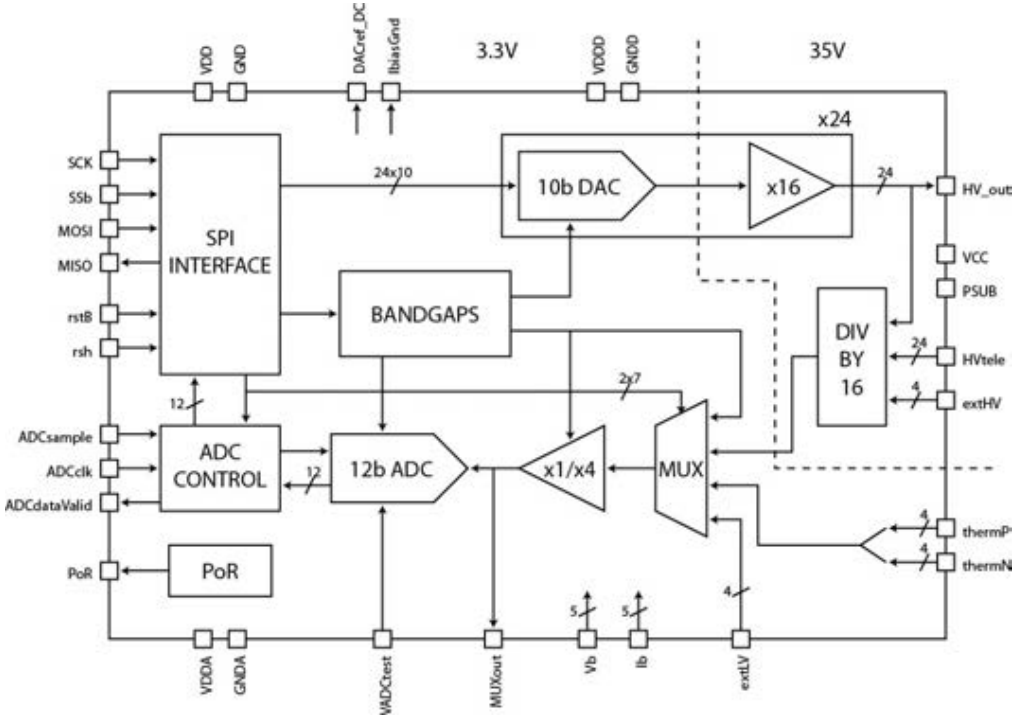
AMS H35 0.35 μm CMOS process

Standard 3.3 V transistors and 50 V high-voltage diffused MOSFET (DMOS) transistors

3.3 V transistors used within the low-voltage interface logic, voltage references and DACs

50 V DMOS transistors to provide the CCD's high-voltage bias supplies directly

High-voltage CCD DC bias ASIC (STAR)



Features

24-channel 10-bit bias voltage outputs

0-32.736 V outputs in 32 mV steps

±20 mA into loads of 10 µF

±25 mA current-limiting short-circuit protection

Housekeeping telemetry system

36-channel housekeeping telemetry system

Multiplexer, variable gain amplifier, 12-bit ADC

General

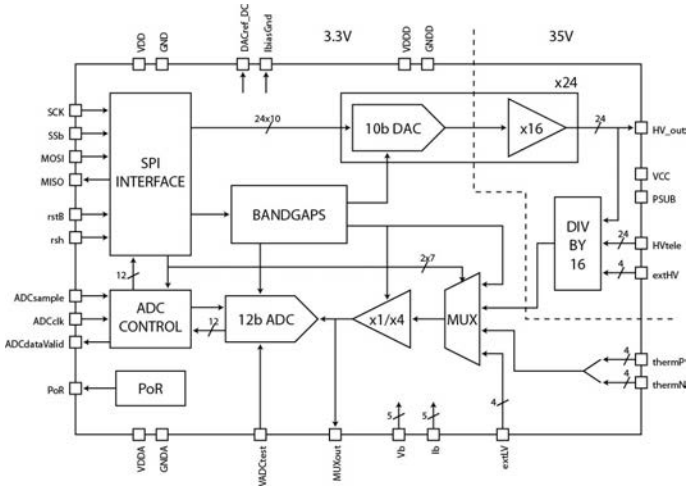
TMR protection against single-event upsets

Guard-ring SEL protected

3.3 V and 35 V supplies

144-pin CQFP

High-voltage CCD DC bias ASIC (STAR)



Performance - characterised -40°C to 125°C

DACs

Output noise	~ 20-40 μV rms (10 μF loading)
Gain accuracy	< 0.3%
Integral non-linearity	< 0.6 LSBs
Quiescent power (at 35 V)	~ 28 mW per DAC

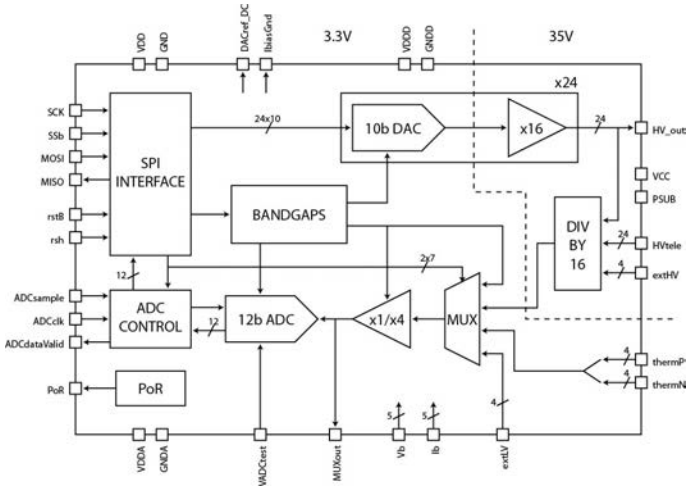
Telemetry system

Integral non-linearity	< 1.3 LSBs
Differential non-linearity	< 0.5 LSBs
Sample noise	< 0.75 LSBs rms

System

Power dissipation:	= 37 mW to 1.17 W (max)

High-voltage CCD DC bias ASIC (STAR)



STAR ASIC

24-channel 10-bit bias voltage outputs with telemetry

36-channel general purpose telemetry system

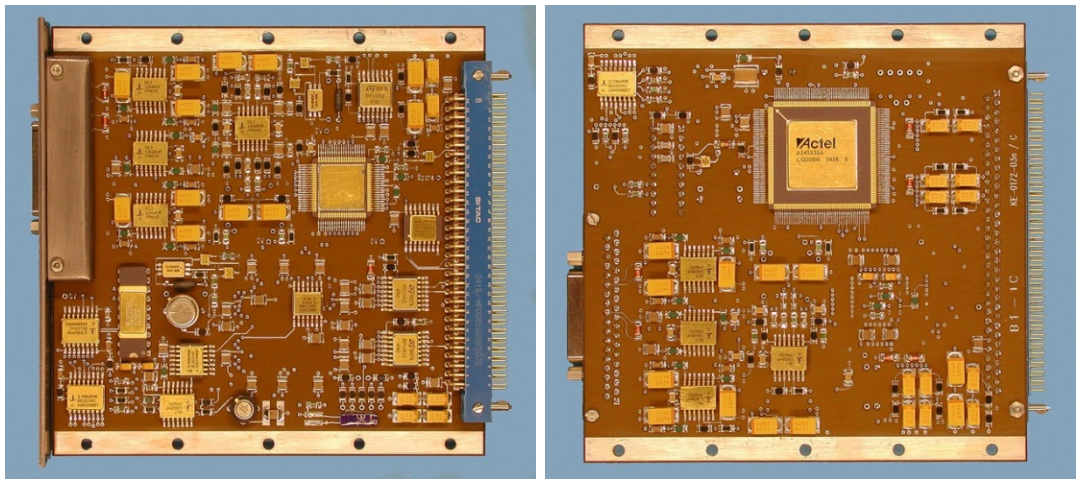
Compared to, or to replace:

SDO bias card

120 mm x 120 mm PCB

7-channel bias voltages set by low-voltage DAC ASIC

16-channel housekeeping and telemetry



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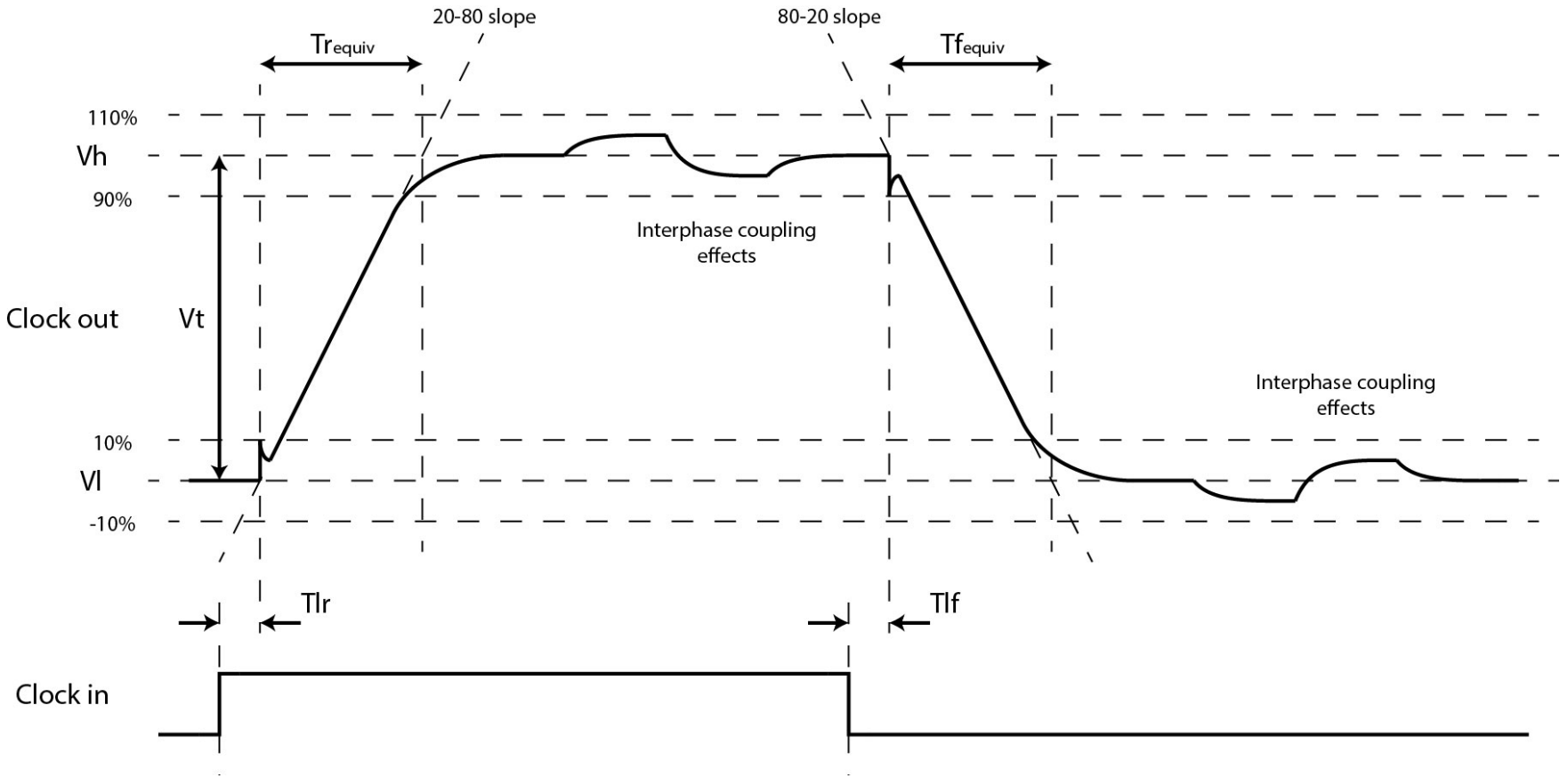
CCD clock driver ASIC (C2BA)

CCD clock driver waveform definition



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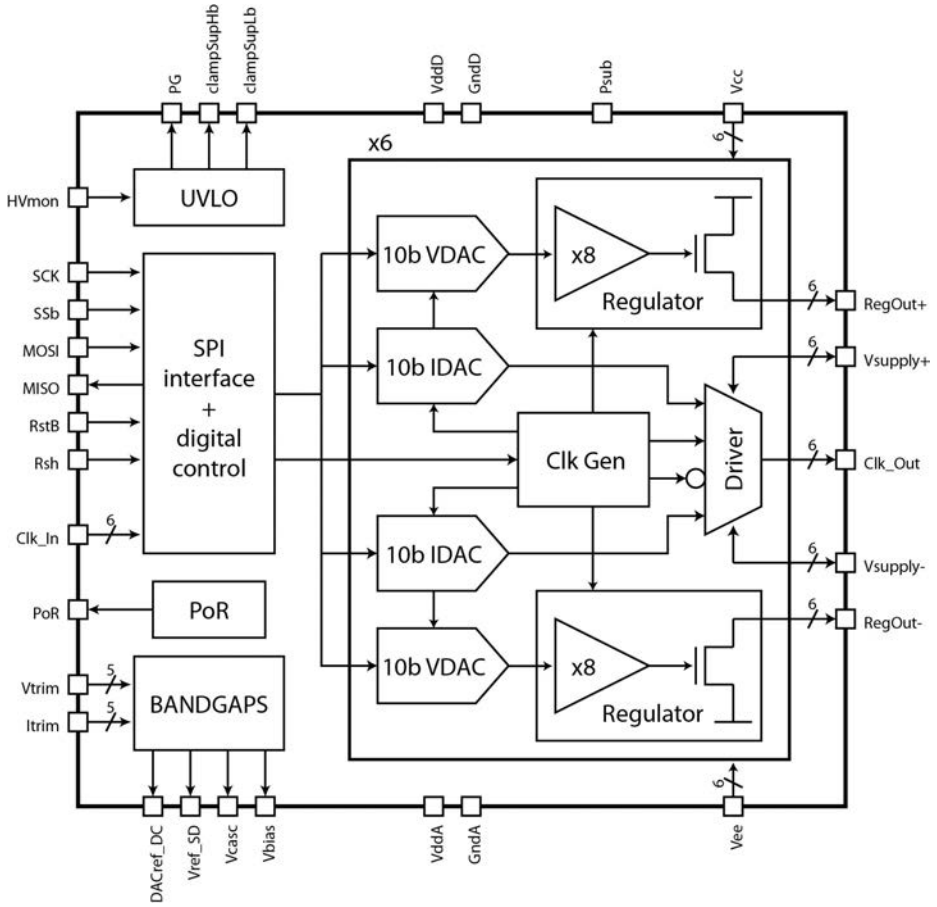
CCD clock driver ASIC (C2BA)



Features

6-channel CCD clock drivers

0-16.368 V outputs in 16 mV steps (each)

0.4-400 mA output drive current (each)

2 pF - 200 nF loads

20 ns - 20 μs Tr / Tf

20-80% linear rise/fall

< ±10% interphase coupling effects

General

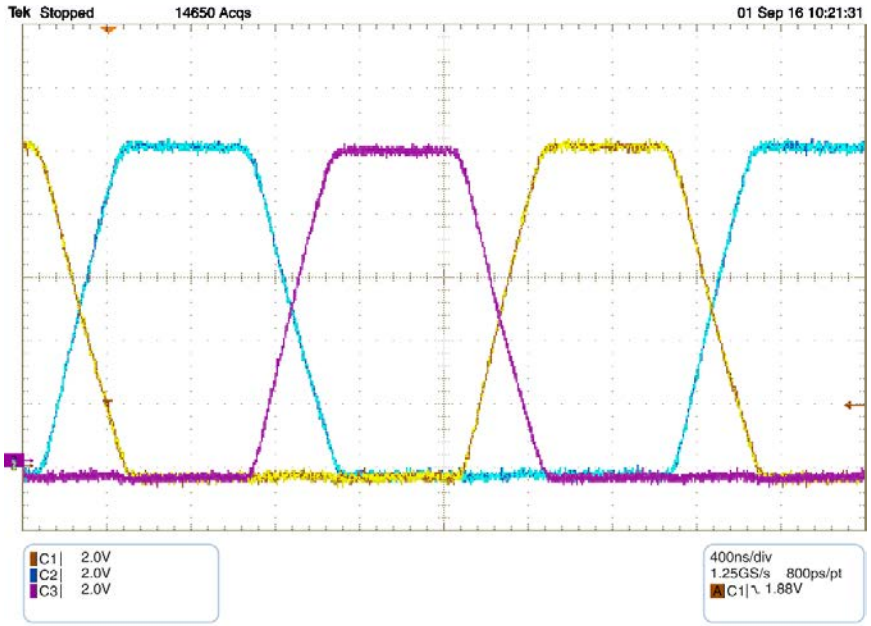
TMR protection against single-event upsets

Guard-ring SEL protected

3.3 V and 18 V supplies

132-pin CQFP

3-phase serial register clocks



120 pF to substrate (0 V)

140 pF interphase coupling capacitance

10 V clock amplitude

1 MHz clocking frequency

50% clock phase overlap

Small interphase coupling seen on the clock-lows

60% clock phase overlap

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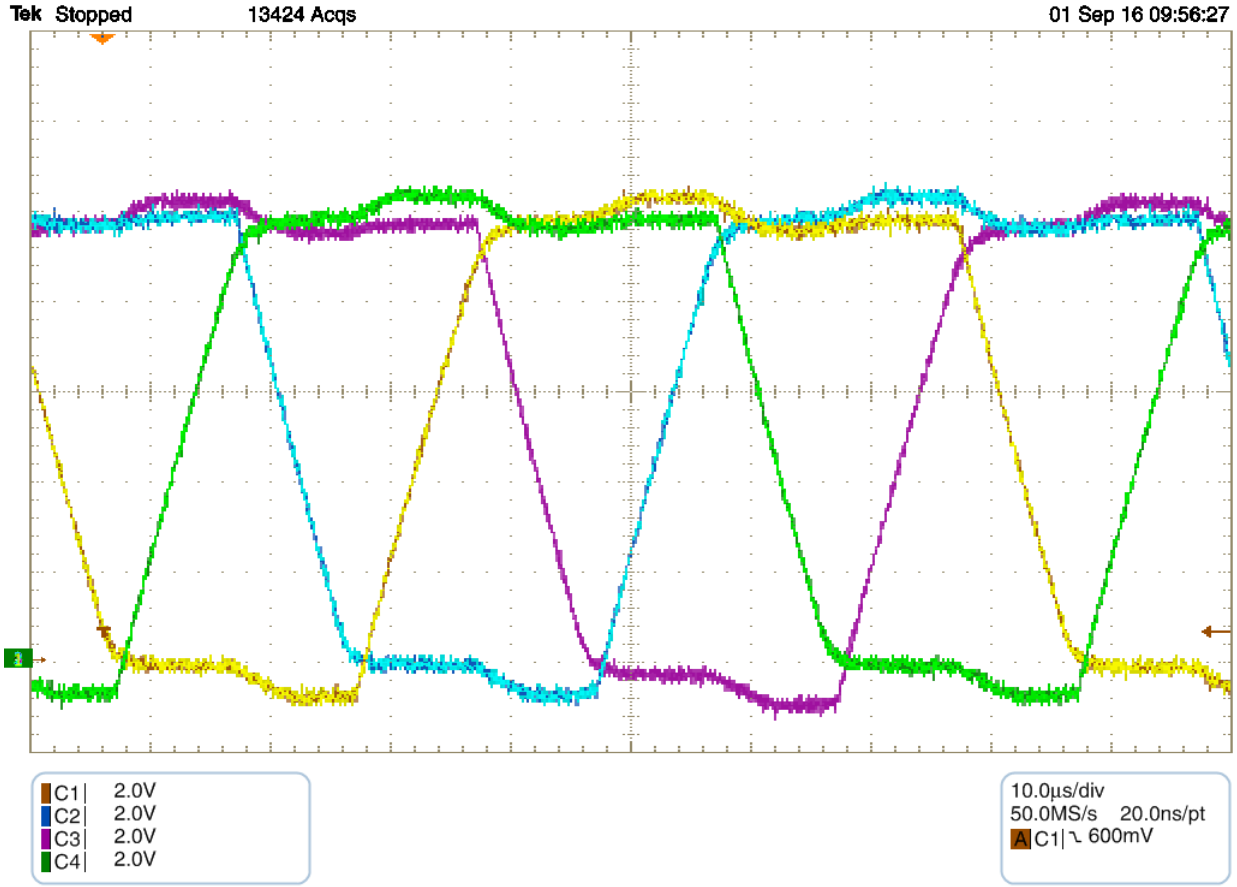
4-phase parallel register clocks



70 nF to substrate (0 V)

16 nF interphase coupling capacitance

10 V clock amplitude

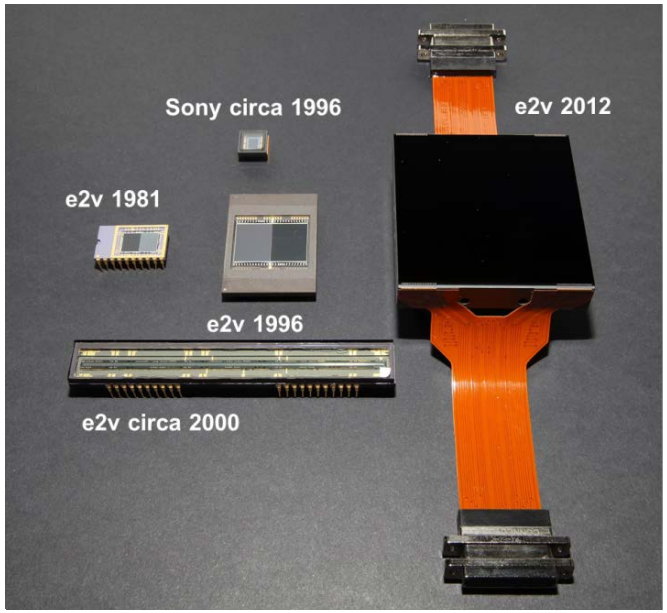
12.5 kHz clocking frequency (80 µs line-transfer time)

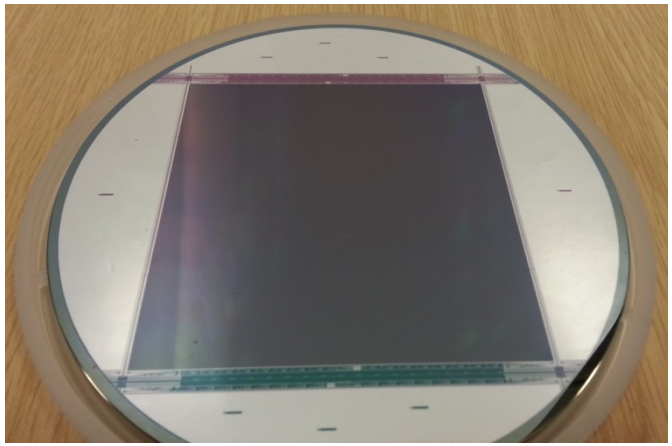
100% clock phase overlap

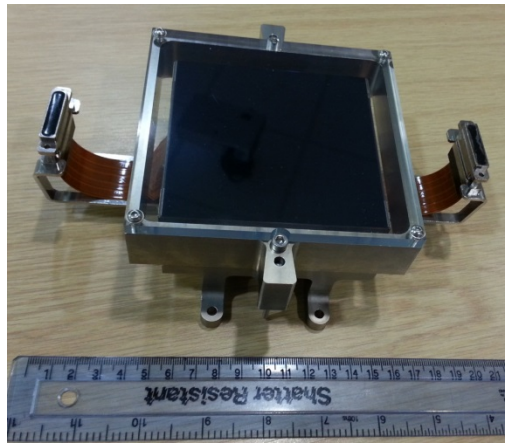
Interphase coupling seen on the clock-lows and clock-highs

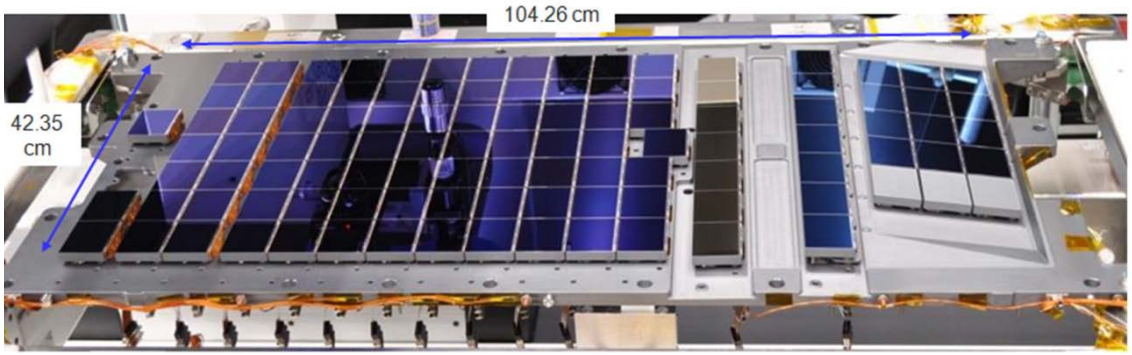
Conclusions and future plans

New challenges in CCD sensors and focal planes









GAIA Focal Plane 106 CCDs ~ 938m pixels ~ 2800 cm2

Kepler Focal Plane 42 CCDs

Conclusions and future plans

Space-borne CCD camera design

- Programme of low- and high-voltage mixed-signal ASIC development
- Radiation-tolerant FPGA(s) for logic-level camera control

Current packaging / qualification of the ASIC die

- Individual die packaged in standard CQFPs

Future packaging / qualification options?

- Multi-die hybrid packaging technologies (multi-chip modules)
- Greater compactness
- Anticipated savings in overall packaging and qualification costs
- Possibly overly-custom and application-specific?
- Concern of impractically high power density?

Increasing sophistication of space-borne CCD camera systems

- Large focal plane arrays of tiled CCDs with multiple video output ports
- Benefits of highly-integrated ASIC functionality and high-density packaging become increasingly attractive and necessary

Thank you for your attention