

The Large Format NIR Detector

**Radiation Testing** 

Peter Knowles Selex ES

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### Large Format NIR ROIC

#### ESA contract 22948 for European alternative to Teledyne Hawaii 2RG arrays

- 0.35 micron CMOS ROIC design for low photon flux and radiation hardness
- Development of 1280x1032, 15 $\mu$ m pitch format NIR (0.8 2.1  $\mu$ m)
- Source Follower in the Detector (SFD) pixels
- Non-destructive reads (NDR) to reduce read noise
- 100ke- full well
- **Power consumption 34mW with 4 outputs, 54mW with 32 outputs**





### Heavy Ion radiation facility at University of Leuven, Belgium

CEOI funding of heavy ion testing of the latest large format ROIC technology for MCT arrays



- Test Facility at the Centre de Ressources du Cyclotron at Louvain-la-Neuve, Belgium
- 10 different heavy ions covering linear energy transfer (LET) from about 1 to 67 MeV cm<sup>2</sup> /mg
- The dose rates can be varied over a wide range, so that a statistically significant number of events can be detected.

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## Heavy Ion Test Campaign





### **Heavy Ion Test Campaign**

- Designed to detect single event effects in both the digital and analogue circuitry
- A range of different effects from memory bit flip to latch up can be assessed
- For each event type, the data will enable characterisation of the LET threshold (level of immunity), saturation cross section (related to the vulnerability at extremely high LET) and the shape of the reliability curve between these points
- Aim to raise 0.35 micron CMOS building blocks from TRL3 to TRL4/5
- Leads to baseline definition of the heavy ion radiation hardness
- Design input to future ROIC designs



### Heavy Ion Species

	Energy (MeV)	Range (µm Si)	Linear Energy Transfer (LET) (MeV cm²/mg)	
M/Q=5 (High LET				
Cocktail)				
<sup>132</sup> Xe <sup>26+</sup>	459	43.0	67.7	
<sup>84</sup> Kr <sup>17+</sup>	316	43.0	40.1	
<sup>40</sup> Ar <sup>8+</sup>	150	42.0	15.9	
<sup>20</sup> Ne <sup>4+</sup>	78	45.0	6.2	
<sup>15</sup> N <sup>3+</sup>	62	64.0	3.3	
M/Q=3.33 (High				
Penetration Cocktail)				
<sup>84</sup> Kr <sup>25+</sup>	756	92.0	31.0	
<sup>59</sup> Ni <sup>18+</sup>	567	98.0	21.3	
<sup>40</sup> Ar <sup>12+</sup>	372	119.0	10.0	
<sup>22</sup> Ne <sup>7+</sup>	233	199.0	3.6	
<sup>13</sup> C <sup>4+</sup>	131	266.0	1.2	



### **Samples and test conditions**

ROICs 50% coated with thin indium to give 2 outputs with grounded and 2 outputs with floating pixels

Room Temperature Indium Coated ROIC

**Cooled Indium Coated ROIC** 

Cooled Thinned CMT Array





**Results Summary** 

Example - digital SEFI on VDD/VDDPIX/VREF supply during high LET test





#### **Results Summary**



#### **Example – digital SEFI cross section**

This type of event is characterised by short transients in the current draw seen by the power supply to chip functions VDD, VDDPIX and VREF.

The sudden current draw on the supply exceeds the capability of the SMU to maintain supply voltage but sufficient supply voltage is maintained to prevent power down of the digital circuits



#### **Results Summary**



These results represent the monitoring of the DUT digital control and therefore the ability for the device to output a valid frame



#### **Results Summary**



#### **Example – frame SEFI cross section**

The test software monitors the frame and line synchronisation outputs and the total number of pixels read out. From this the software determines if the frame is valid or not and records the result.



### **Results Summary**

		Digital SEU	Frame SEFI	Digital SEFI	Analogue SEFI	Analogue SET	Analogue SEU
Room Temperature ROIC	LET <sub>th</sub>	11	9	11	8	7	9
with 50% metal Coat	Sat	6.00E-05	2.00E-05	3.00E-04	7.00E-05	1.50E-05	4.00E-05
Cooled ROIC with 50% metal	LET <sub>th</sub>	11	9	11	8	7	9
Coat	Sat	5.00E-05	1.20E-05	2.00E-04	7.00E-05	9.00E-06	4.00E-05
Cooled MCT Hybridised	LET <sub>th</sub>	11	9	11	8	7	9
ROIC	Sat	5.00E-05	1.20E-05	2.00E-04	5.00E-05	9.00E-06	1.00E-05

LET<sub>th</sub> : Threshold value (MeV cm<sup>2</sup>/mg) Sat : Saturated cross-section (cm<sup>2</sup>)

#### **Definition of Events**

SEL	Single event latch-up; defined as the DUT drawing excess current.		
Digital SEU	Bit flip in digital memory		
Frame SEFI	Incorrect array read out. Can be due to incorrect number of pixels or incorrect		
	sync op signals output by ROIC resulting in the read out array being incorrectly		
	formed into a 2D image.		
<b>Digital SEFI</b>	Anomalous current draw via the ROIC digital supplies		
Analogue	Anomalous current draw via the ROIC analogue supply		
SEFI			
Analogue	Glitch in analogue output		
SET			
Analogue	Sampled glitch in the pixel resulting in a read out pixel having the wrong voltage.		
SEU			



### **Results Summary**

No latch-up (SEL) observed demonstrating good immunity and reduced risk of permanent damage

⇒ Recovery of Frame SEFI occurs after reset

⇒ Other events can be managed



### **Results Summary**

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#### **BCY70** Temperature sensor

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